The Report committee for Sarvesh Ganesan

Certifies that this is the approved version of the following report

Area, Delay and Power Comparison of Adder Topologies

APPROVED BY SUPERVISING COMMITTEE:

Supervisor: _____

(Earl E. Swartzlander, Jr.)

_____

(Nur Touba)

Area, Delay and Power Comparison of Adder Topologies

by

Sarvesh Ganesan, B.Tech.

Report

Presented to the Faculty of the Graduate School

of the University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

December, 2015

Acknowledgements

First of all, I want to thank Amma and Appa (my parents) for their constant support and giving me all the freedom required to choose my own academic and career paths. They have always been there for me, providing the encouragement and motivation to help me reach the next level.

I would like to sincerely express my gratitude to my supervisor, Dr. Earl E. Swartzlander, Jr. for accepting to provide his guidance and valuable inputs for completing this report. It has been a great experience interacting with him during his lectures as well as while working for this report. I would also like to thank my co-supervisor, Dr. Nur Touba, for providing his inputs and suggesting the required changes to make the report as valuable and informative as possible.

I would also like to thank my project partner Ankith G. Shanthiraj for all his help in completing the work and this report.

Lastly, I am indebted to my former colleagues at Synopsys India Private Limited, Hyderabad, India especially my Managers, Harish Balan and Deepak Ninnar for their constant support and belief in me, and my team mates Mahesh Narayan, Bhaskar Chintapalli, Payal Deb, Indu Syamala and Madhu Kandi for sharing their knowledge on the flow and usage of various CAD tools.

Area, Delay and Power Comparison of Adder Topologies

by

Sarvesh Ganesan, MSE

The University of Texas at Austin, 2015

SUPERVISOR: Earl E. Swartzlander, Jr.

An adder is an indispensable component for a processing system and is ever-present on an integrated circuit. With scaling and the increasing levels of integration seen in the contemporary integrated circuits, power consumption has become an important factor in deciding the performance of any adder circuit in addition to the speed. Area has always been another factor which is taken into account based on the application.

This work provides a comprehensive analysis of the standard cell based CMOS implementations of six adder topologies of different word sizes in 45nm technology. The analysis is done on leakage power, dynamic power, speed and area. The switching activities of the circuits were captured using dynamic gate level simulation to perform the time based peak power analysis. Static timing analysis was performed to estimate the delay of the critical path for each circuit. The complexity of the circuit is decided based on the number of gates used in the implementation and the area utilized by the standard cells in the circuit.

The analysis and results presented in this report will be helpful in choosing a specific adder configuration for an integrated circuit based on the constraints related to its application.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Importance of Adders

The addition circuitry forms the basic core of the ALU of processing cores and its efficiency and performance is critical to the overall system. Consequently, over the years, a significant amount of research has gone into designing low-latency adder topologies by primarily cutting down on the carry propagation delay [1] [2] [3]. These efforts led to the design of the parallel prefix computation method for fast carry propagation [4]. Various configurations were implemented among parallel-prefix adders offering trade-offs between the complexity (area) and delay [7] with [5] and [6] being the end cases of this family of adders. Numerous attempts have been made to develop hybrid schemes using a combination of the above mentioned adders and trade speed for area, or power for speed. The carry select and carry skip versions have been extensively studied and optimized in [8] [9] and [10].

Previous attempts to estimate energy consumption in VLSI circuits have used probabilistic methods based on logic transitions averaged over a large data set fed in as input vectors [11]. The parallel prefix versions have been studied similarly in [12]. Further, a particular VLSI implementation can use static or dynamic CMOS where logic function is usually packed into a complex logic blocks. Thus, the notion of logic gate and associated gate delay becomes artificial and misleading.

1.2 Problem Description

Selection of an initial topology for an adder to yield a circuit which meets the required performance specifications is one of the most important steps in the design. The actual performance parameters are known only at the time of simulation or analysis after the implementation. Going back and forth between the implementation choices will be

time consuming. This work targets to eliminate the iteration involved in the selection of an adder topology by providing a preliminary analysis of the various adder configurations across several adder sizes. The performance parameters analyzed are delay, power and area.

1.3 Overview of the Analysis

The analysis performed in this work evaluates the use of the logical effort method not only for the purpose of better delay estimations but also for evaluation of different adder topologies and their impact on design of VLSI adders [13]. A more direct approach to computing the power consumption is done with the help of all the advanced tools that are currently available.

However, with the advancement of technology, parasitic components are increasingly playing a dominant role and interconnects are becoming the bottleneck for speed. In the light of these design concerns, the aim is to estimate the delay and power and compare them with existing adder topologies and investigate if the established trends still hold well as scaling impacts the IC realm. Increasing emphasis is being placed simultaneously on power efficiency and speed. Design-tradeoffs are omnipresent and performance parameters are set based on the application needs. Keeping speed in mind, the Kogge-Stone and Ladner-Fischer parallel prefix adders are used for comparison with the Carry Look Ahead, Carry Select, Carry Skip and the traditional Ripple Carry adders. A modified version of the Ladner-Fischer PPA trading off fan-out for delay is implemented to investigate its feasibility for different adder sizes.

1.4 Exploration of Subthreshold Operation

Finally, for low speed applications where energy consumption is the primary concern, subthreshold implementation of adder circuits is explored [14]. Kogge-Stone PPA, one that offers the best speed, is tested for sub-threshold logic and the results are tabulated. Signal integrity and noise play a significant role in sub-threshold circuits and thus as a preliminary test, an 8-bit Kogge-Stone adder is tested.

Chapter 2: Approach and Design Methodology

2.1 Configurations Considered and the Design

Six different adder configurations were considered for the analysis, namely Ripple Carry adder, Carry Select adder, constant width Carry Skip adder, Carry Look Ahead adder, and the two parallel prefix adder configurations, Kogge-Stone and Ladner-Fischer. Three different adder sizes; 8, 16 and 32 bits were considered for each configuration.

The design of the adders was performed using the Cadence Virtuoso Schematic Editor using only three different standard cells, NAND(two-input), NOR(two-input) and INVERTER(size=1x and size=4x). The standard cells used for the design were characterized at 45nm technology with the operating conditions of 1V and 27^{o}C.

The Verilog netlist was generated from Virtuoso so that this could be used for further analysis and for Automatic Placement and Routing.

2.2 Verification and Activity File Generation for Power Analysis

For the gate level simulation, a particular set of pseudo random input vectors, written as a Verilog testbench were provided to each of the 6 adder configurations for a given word size. The functional correctness of each of the adder configurations was verified. The simulation was also helpful in dumping the states of the internal nodes of the design for a given simulation time. This is used for the peak power analysis. The CAD tool used for the gate level simulation is Synopsys VCS and the states of the internal nodes of the circuit are dumped in the file format .vcd.

The vcd file dumped by VCS is taken into the Synopsys power analysis tool, Primetime-PX for performing the time based peak power analysis. Primetime-PX reads in the design in the form of Verilog Netlist generated from Cadence along with the 45nm

standard cell library in the Synopsys .db format. The library contains the tables of the characterized values of internal energy per transition. It also contains the state and path dependent leakage power numbers for each cell. The resultant waveforms generated are in the .fsdb format and have been plotted using the Synopsys Cosmoscope waveform tool. The waveforms provide a histogram of the peak power values at each point of time where there is a change in input vectors. The peak power values include the leakage power and the dynamic power at the particular time stamps.

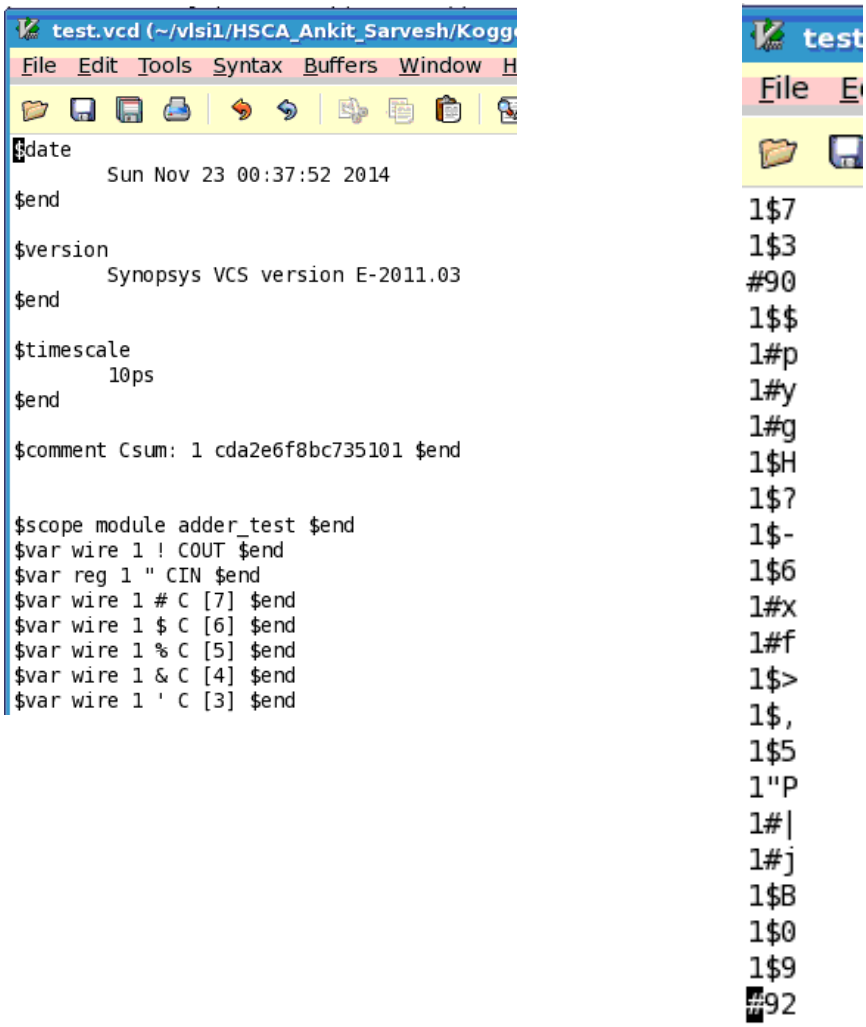

Fig 1: Snippet of a vcd file with Symbols Assigned to Nets and the Value at the Time Stamp.

2.3 Estimation of Critical Delay Using Static Timing Analysis

For the pre-layout static timing analysis, Synopsys STA tool, Primetime was used to estimate the delay of the critical path of each circuit. The cell delay and the transition tables in 45nm standard cell library for the NAND, NOR and the INVERTER cells were considered in the calculation. For measuring the interconnect delays, wire load models present in the libraries were used.

For the post-layout static timing analysis, the SPF file generated from encounter after the placement and routing was used instead of the wire load models to generate more realistic delay values of the critical paths.

2.4 Physical Design – Placement and Routing

The physical design of each of the configurations was generated using Cadence Encounter. The LEF file was provided for the 45nm standard cell technology node along with the layer geometry information. Automatic placement and routing with pre-place and in-place optimization was performed to generate a layout without any design rule violations or functionality changes. The parasitic extraction was then performed to generate the SPF file which models the cell and interconnect delays as RC networks. This file helps in generating a more realistic delay values compared to the pre layout delay values estimated above.

For estimating the complexity and area, the number of gates (NAND, NOR and INVERTER) are measured using the Synopsys synthesis tool Design Compiler. The physical area of the chip after placement and routing was generated from Cadence Encounter.

2.5 List of EDA Tools Used for Design and Analysis

1. Synopsys VCS: Synopsys VCS is an RTL functional simulator that can simulate Verilog, VHDL, and System C models. It was used to verify the functionality of the

structural netlists generated from Synopsys Design Compiler or Cadence Virtuoso Schematic editor. This tool was also used in generating the vcd files for peak power analysis.

2. Synopsys Design Compiler: DC is a synthesis tool. It maps a behavior model of a design (RTL hardware description model) using a standard cell library into a gate-level netlist.

3. Cadence Virtuoso Schematic Editor: This editor was used to describe the connectivity between standard cells using GUI.

4. Cadence Encounter: This tool was used to perform automatic placement and routing. The input to this tool will be a synthesized gate level netlist. The output is a placed and routed design.

5. Mentor Graphics Caliber: This tool was used to perform DRC and LVS checks after placement and routing and extract the parasitics for accurate timing and power analysis post-layout.

6. Synopsys Primetime: Synopsys PrimeTime is the industry standard tool for timing sign-off. It delivers accurate timing signoff analysis that helps pinpoint timing problems prior to tapeout.

7. Synopsys Primetime-PX: PT-PX analyzes static and dynamic power based on the activity file which provides the static probability and toggle rate information.

8. Synopsys Cosmoscope: Viewing the peak power waveforms dumped by PT-PX in **.fsdb** format.

Chapter 3: Optimization Steps

1. Logical effort theory and back-of-the-envelope calculations were used to analyse the critical path and ensure appropriate buffering and driver sizes to drive large loads reducing the stage effort and consequently the overall delay as well. Inverters of two different drive strengths were used selectively to buffer loads off the critical path as well as high fan-out nodes.

2. Since there was a restriction in the usage of standard cells to just NAND2X1, NOR2X1, INVX1 and INVX4, logical effort theory went into the design of the XOR gates, prefix blocks and other such higher level blocks used repetitively.

3. Auto-place and route in Cadence Encounter was performed iteratively with different floorplans and optimization constraints to achieve a layout that would occupy the least area on the chip while ensuring appropriate routing resources are available within the module.

4. Only the least stage implementations of the prefix adder family in Kogge-Stone and Ladner-Fischer were investigated. However, the possibility of fanout impacting the performance negatively even with large buffers was a drive to tweak the topology to extend it to 5 stages and analyze if it would give a better performance for higher adder sizes. Fig 2 shows the tree adder structures.

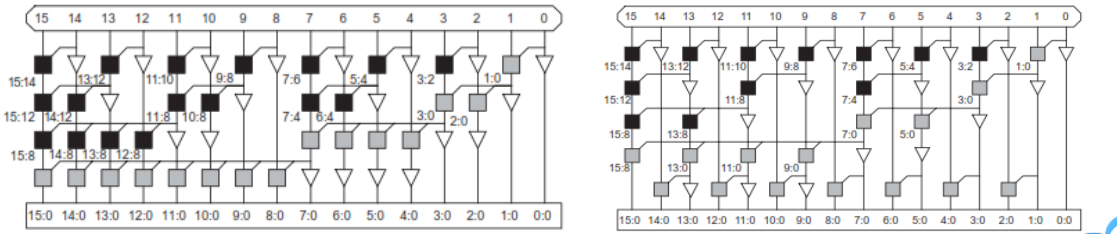

Fig 2: Ladner-Fischer 16 bit (left) and Modified Ladner-Fischer 5 stage (right)

5. Peak power analysis was performed instead of the traditional average power analysis. The time-based peak power analysis is advantageous in the fact that the switching activity values (namely the static probability and the toggle rate) are not averaged over the entire simulation time. Instead, the logical states of all the nets in the design have been dumped using gate level simulation in the form of an activity file (vcd). This vcd file is later used for the calculation of dynamic and leakage power at each instance of time based on the real time of input vectors.

   Time based peak power analysis helps in understanding the peak power consumption of the circuit and the input vectors which tend to cause the highest power consumption. The peak power waveform results for all adder configurations of different sizes are shown in Section 4.2.3.

6. The previous work carried out in the area of performance comparisons have been restricted to the traditional adder topologies and the three parallel prefix adder topologies. This work provides a comprehensive comparison between the broader ranges of adder topologies from traditional ripple carry adders to the faster parallel prefix adders such as the Kogge-Stone implementation.

7. The delay values calculated for the critical paths include the interconnect delays calculated using the RC delay models.

The SPEF file generated after placement and routing creates the lumped RC network models of all the nets in the design. This rigorous method will help understand the overhead in the critical path delay due to the net length in addition to the logical depth seen in the path.

Most of the delay comparisons performed in the previous work have been theoretical and used the logic effort model or the wire load models which may not be as accurate as the post layout delay values used in our work.

For example, in the case of Ladner-Fischer configuration, the net length plays an important role in the critical path delay. This is a lot more evident in the 32-bit configuration in the corresponding post layout delay table.

Chapter 4: Results of Comparison of Adder Topologies

4.1 Comparison of the Critical Path Delay

4.1.1 Pre-Layout Primetime Results

Table 1: Comparison of Pre-Layout Delay Performance (in ns)

Adder Type	Pre-Layout Delay (in ns)		
	8 bits	16 bits	32 bits
Kogge-Stone	0.3	0.36	0.41
Ladner-Fischer	0.35	0.45	0.61
Modified Ladner-Fischer	0.37	0.46	0.58
Ripple Carry	0.56	1.05	2.04
Carry Look Ahead	0.4	0.52	0.72
Carry Select	0.39	0.55	0.78
Carry Skip	0.42	0.6	0.87

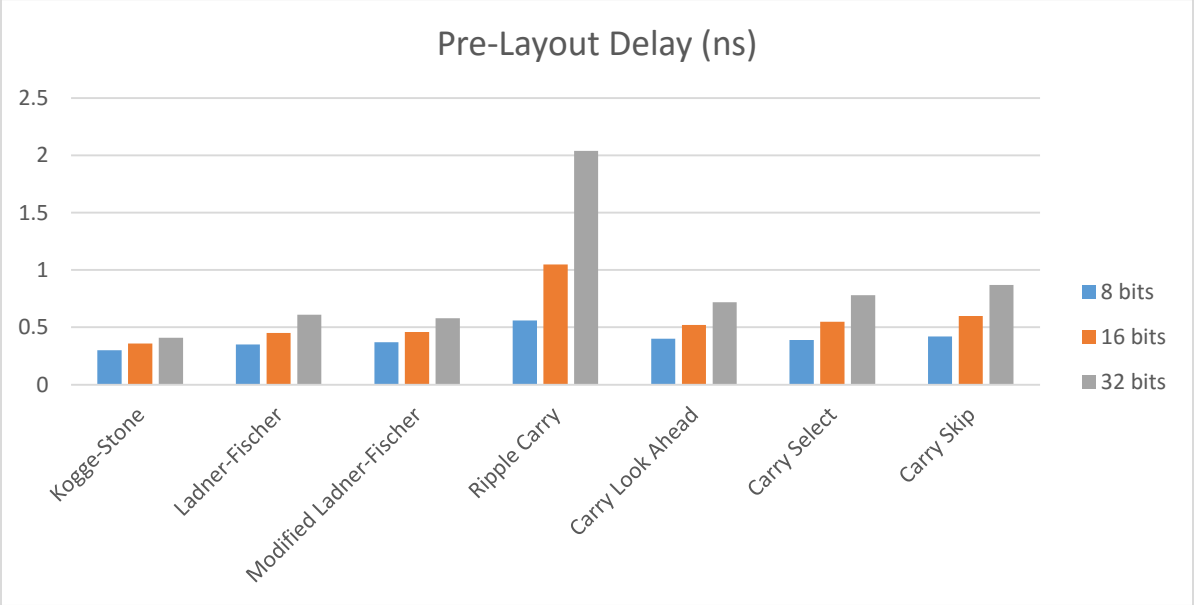

Fig 3: Pre-Layout Delay for the Adder Topologies for 8, 16 and 32 Bit Sizes

4.1.2 Post-Layout Primetime Results

Table 2: Comparison of Post-Layout Delay Performance (in ns)

Adder Type	Post _Layout Delay(ns)		
	8 bits	16 bits	32 bits
Kogge-Stone	0.33	0.42	0.49
Ladner-Fischer	0.38	0.51	0.71
Modified Ladner-Fischer	0.41	0.52	0.68
Ripple Carry	0.62	1.14	2.23
Carry Look Ahead	0.42	0.59	0.83
Carry Select	0.41	0.6	0.85
Carry Skip	0.47	0.65	0.96

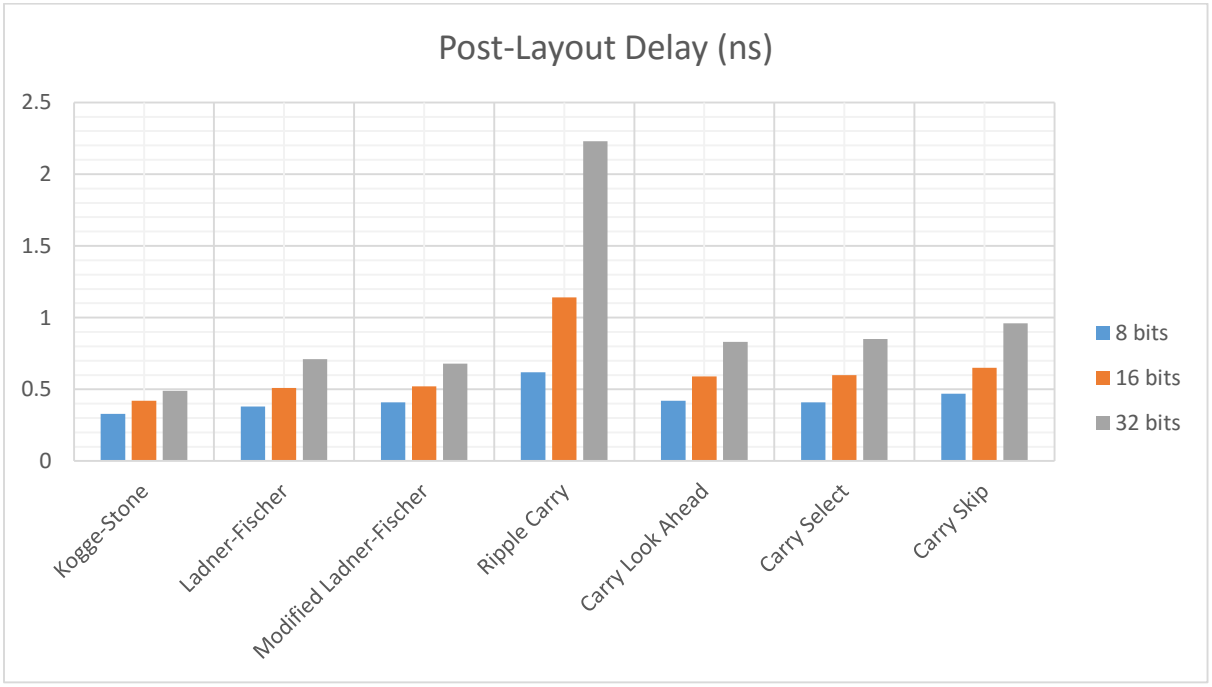

Fig 4: Post-Layout Delay for the Adder Topologies for 8, 16 and 32 Bit Sizes

4.2 Power Analysis and Comparison

4.2.1 Peak Power Comparison

Table 3: Peak Power Response of the Adder Topologies (in mW)

Type of Adder	Peak Power(mW)		
	8 bits	16 bits	32 bits
Kogge-Stone	7.109	14.13	25.1
Ladner-Fischer	7.067	14.5	23.3
Modified Ladner-Fischer	7.226	14.5	22.6
Ripple Carry	2.909	5.644	8.157
Carry Look Ahead	4.733	9.245	15.2
Carry Select	5.32	10.1	16.8
Carry Skip	5.175	10.2	15

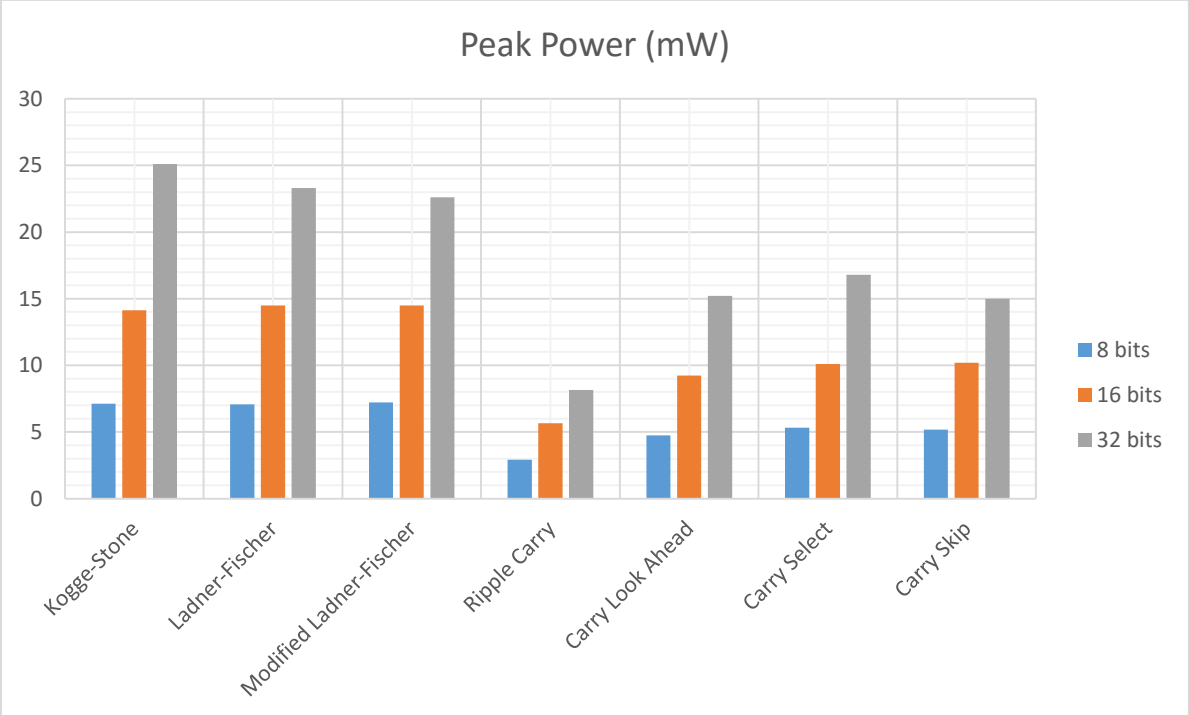

Fig 5: Peak Power Comparison for the Adder Topologies for 8, 16 and 32 Bit Sizes

4.2.2 Average Power Comparison

Table 4: Total Average Power Response of the Adder Topologies (in µW)

Adder Type	Total Avg. Power(uW)		
	8 bits	16 bits	32 bits
Kogge-Stone	4.441	9.06	20.21
Ladner-Fischer	4.159	8.275	18.56
Modified Ladner-Fischer	4.067	7.674	16.52
Ripple Carry	1.381	2.682	5.796
Carry Look Ahead	2.825	4.267	8.898
Carry Select	2.963	5.722	13.96
Carry Skip	2.333	4.392	9.021

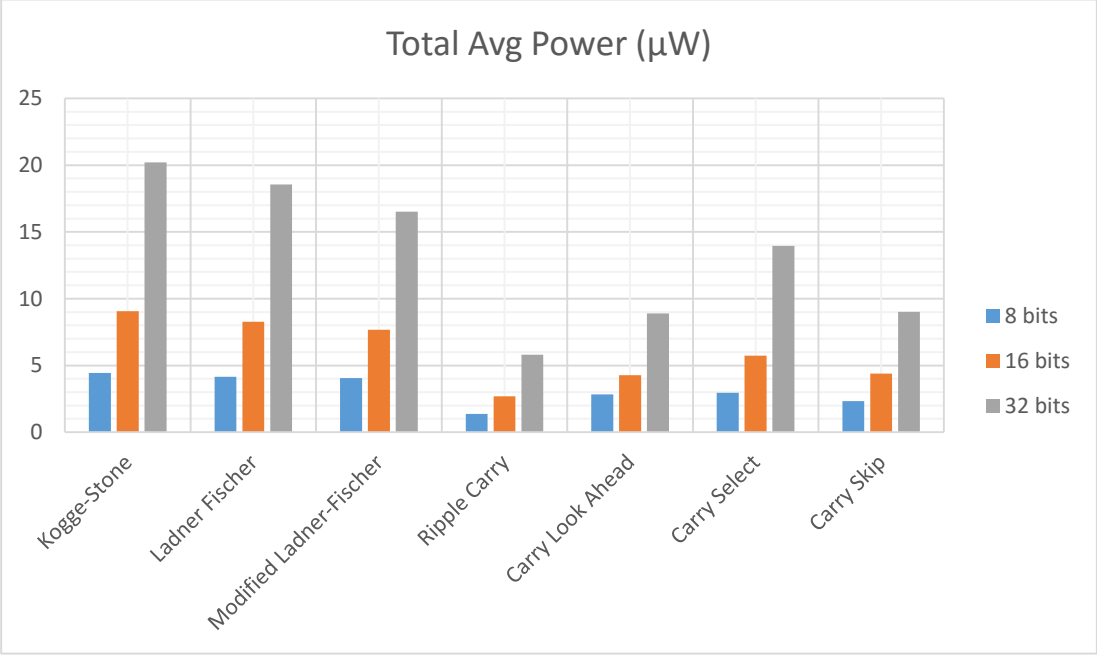

Fig 6: Total Average Power Comparison for the Adder Topologies for 8, 16 and 32 Bit Sizes

4.2.3 Peak Power Waveform Results (All Configurations and Sizes)

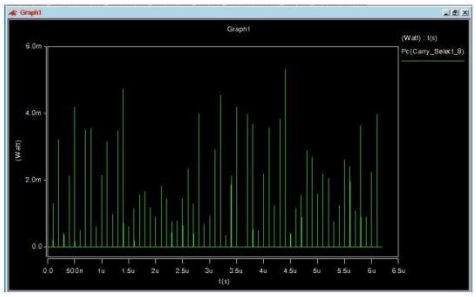

Fig 7.1a: Peak Power Waveform, Carry Select Adder (8-bit)

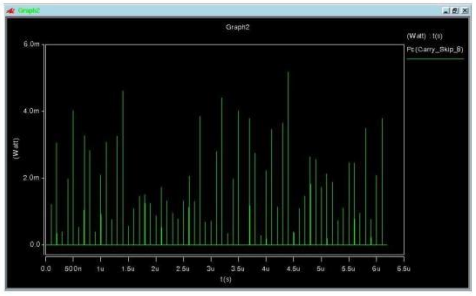

Fig 7.2a: Peak Power Waveform, Carry Skip Adder (8-bit)

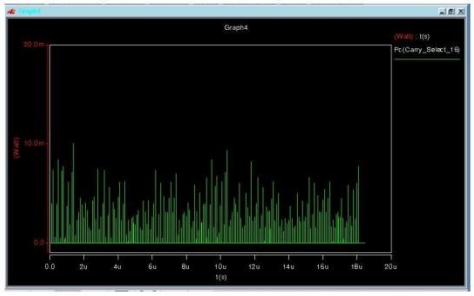

Fig 7.1b: Peak Power Waveform, Carry Select Adder (16-bit)

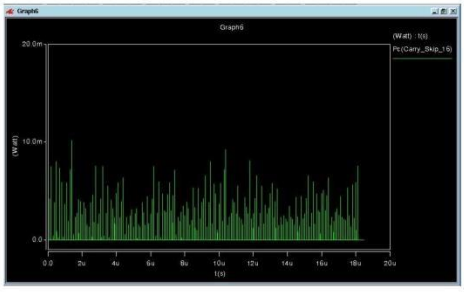

Fig 7.2b: Peak Power Waveform, Carry Skip Adder (16-bit)

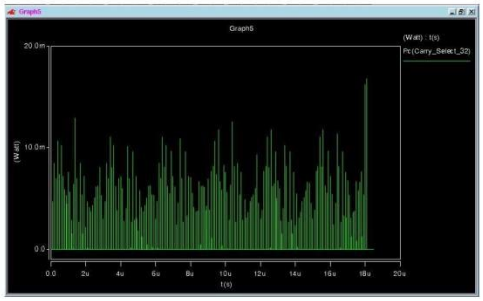

Fig 7.1c: Peak Power Waveform, Carry Select Adder (32-bit)

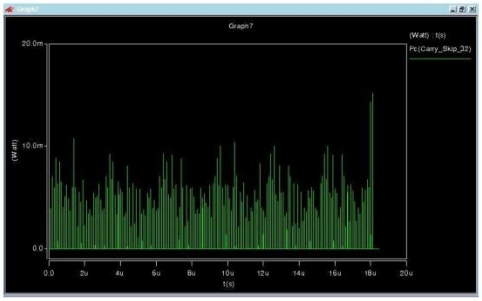

Fig 7.2c: Peak Power Waveform, Carry Skip Adder (32-bit)

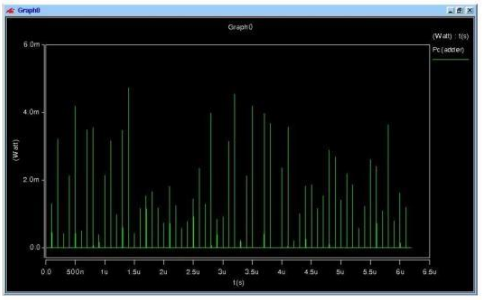

Fig 7.3a: Peak Power Waveform, Carry Look Ahead Adder (8-bit)

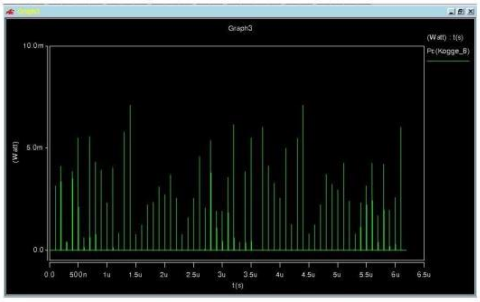

Fig 7.4a: Peak Power Waveform, Kogge-Stone Adder (8-bit)

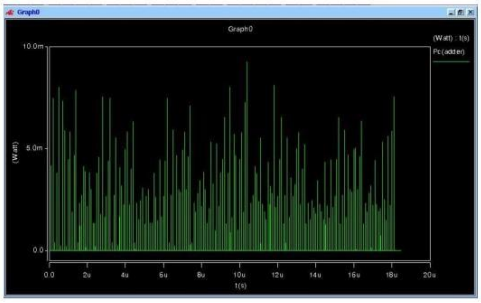

Fig 7.3b: Peak Power Waveform, Carry Look Ahead Adder (16-bit)

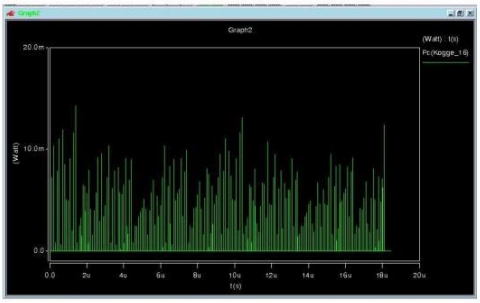

Fig 7.4b: Peak Power Waveform, Kogge-Stone Adder (16-bit)

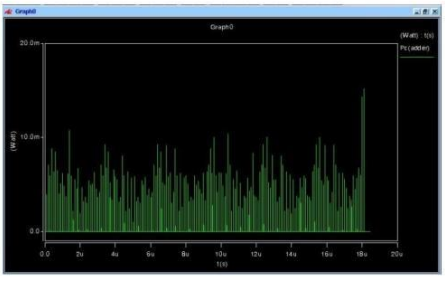

Fig 7.3c: Peak Power Waveform, Carry Look Ahead Adder (32-bit)

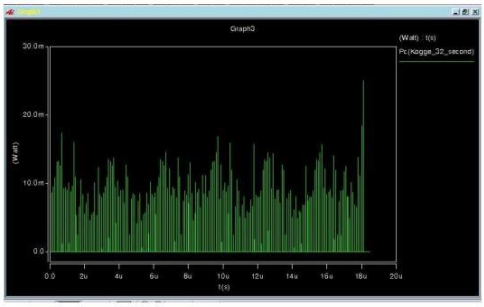

Fig 7.4c: Peak Power Waveform, Kogge-Stone Adder (32-bit)

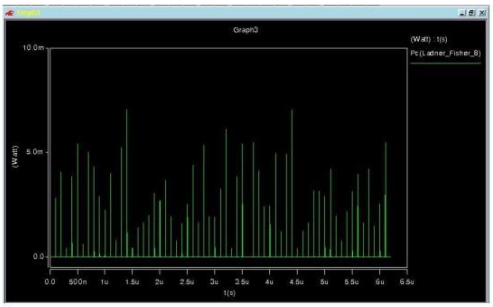

Fig 7.5a: Peak Power Waveform, Ladner-Fischer (8-bit)

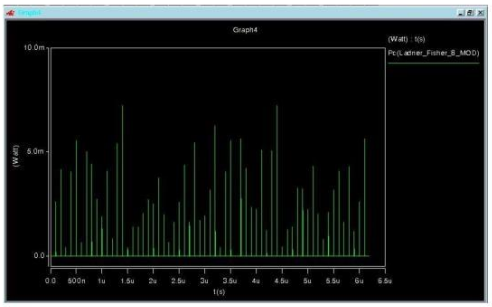

Fig 7.6a: Peak Power Waveform, Modified Ladner-Fischer (8-bit)

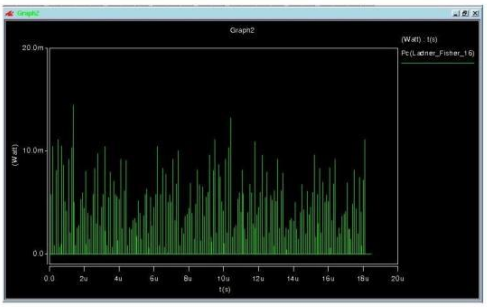

Fig 7.5b: Peak Power Waveform, Ladner-Fischer (16-bit)

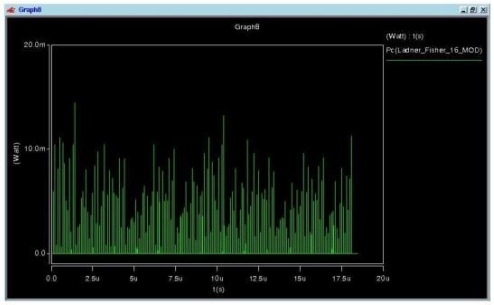

Fig 7.6b: Peak Power Waveform, Modified Ladner-Fischer (16-bit)

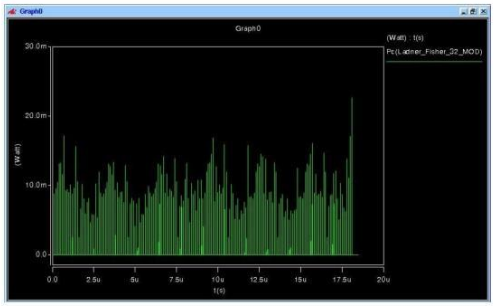

Fig 7.5c: Peak Power Waveform, Ladner-Fischer (32-bit)

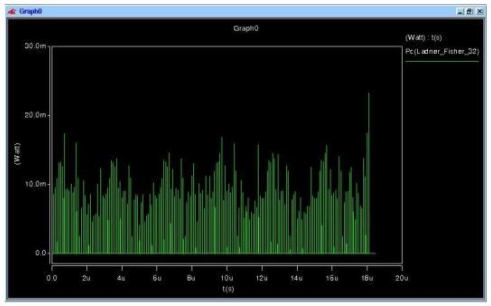

Fig 7.6c: Peak Power Waveform, Modified Ladner-Fischer (32-bit)

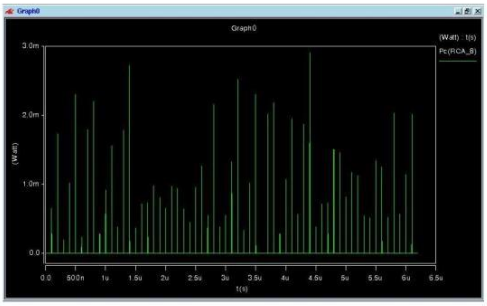

Fig 7.7a: Peak Power Waveform, Ripple Carry Adder (8-bit)

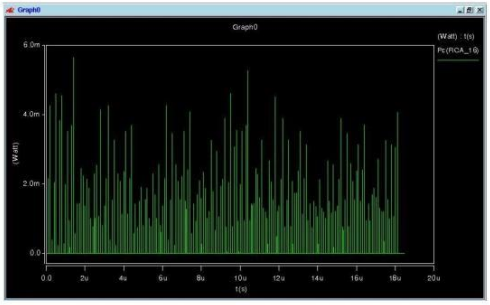

Fig 7.7b: Peak Power Waveform, Ripple Carry Adder (16-bit)

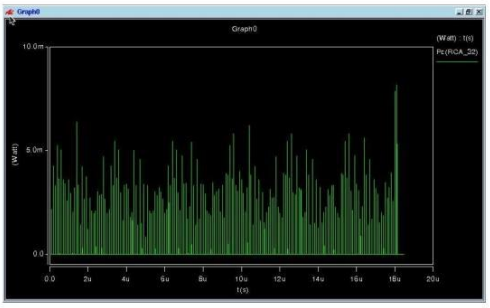

Fig 7.7c: Peak Power Waveform, Ripple Carry Adder (32-bit)

4.3 Area Comparison

Table 5: Total Area of the Adder Topologies (in μm^2)

Type of Adder	Area (in μm^2)		
	8 bits	16 bits	32 bits
Kogge-Stone	442.08	1005.7	2254.98
Ladner-Fischer	412.98	912.788	1993.117
Modified Ladner-Fischer	405.005	854.59	1792.25
Ripple Carry	142.66	285.33	570.67
Carry Look Ahead	242.62	626.04	1360.50
Carry Select	310.2	610.55	1387.25
Carry Skip	175.3	445.7	780.28

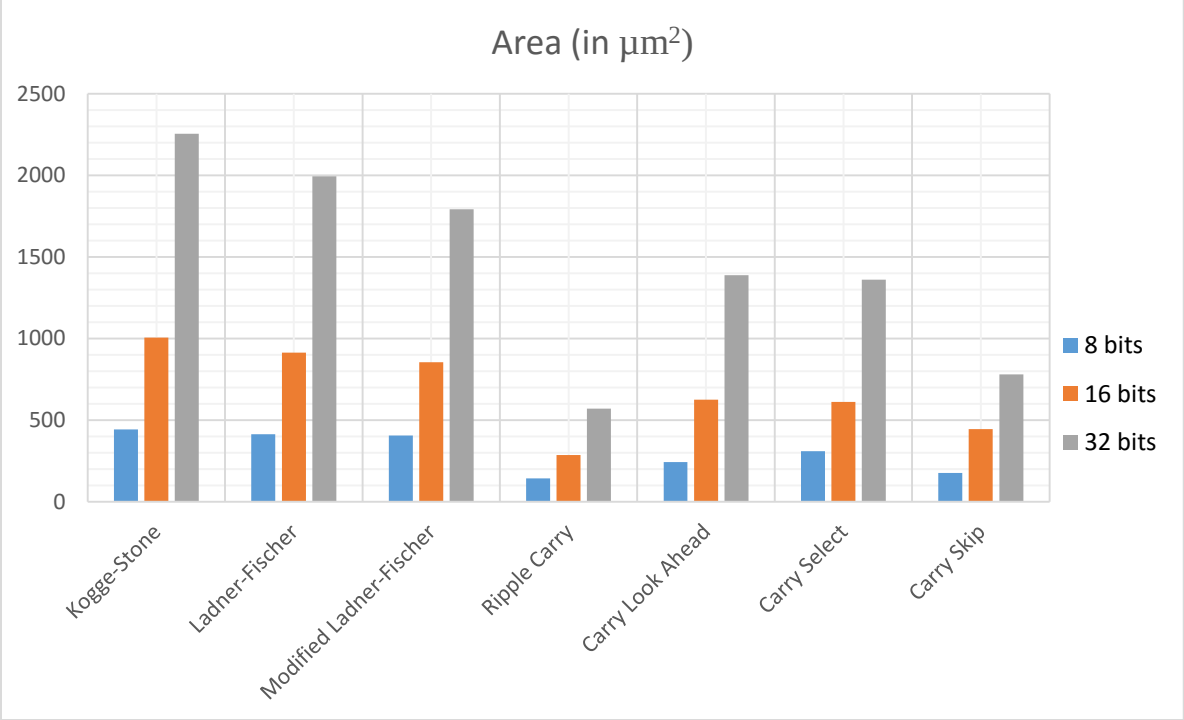

Fig 8: Total Area comparison for the Adder Topologies for 8, 16 and 32 Bit Sizes

4.4 Complexity: Total Number of Gates

Table 6: Total Complexity of the Adder Topologies

Type of Adder	Complexity (Number)		
	8 bits	16 bits	32 bits
Kogge-Stone	265	600	1354
Ladner-Fischer	248	543	1177
Modified Ladner-Fischer	246	520	1090
Ripple Carry	72	144	288
Carry Look Ahead	129	339	737
Carry Select	160	314	700
Carry Skip	76	154	316

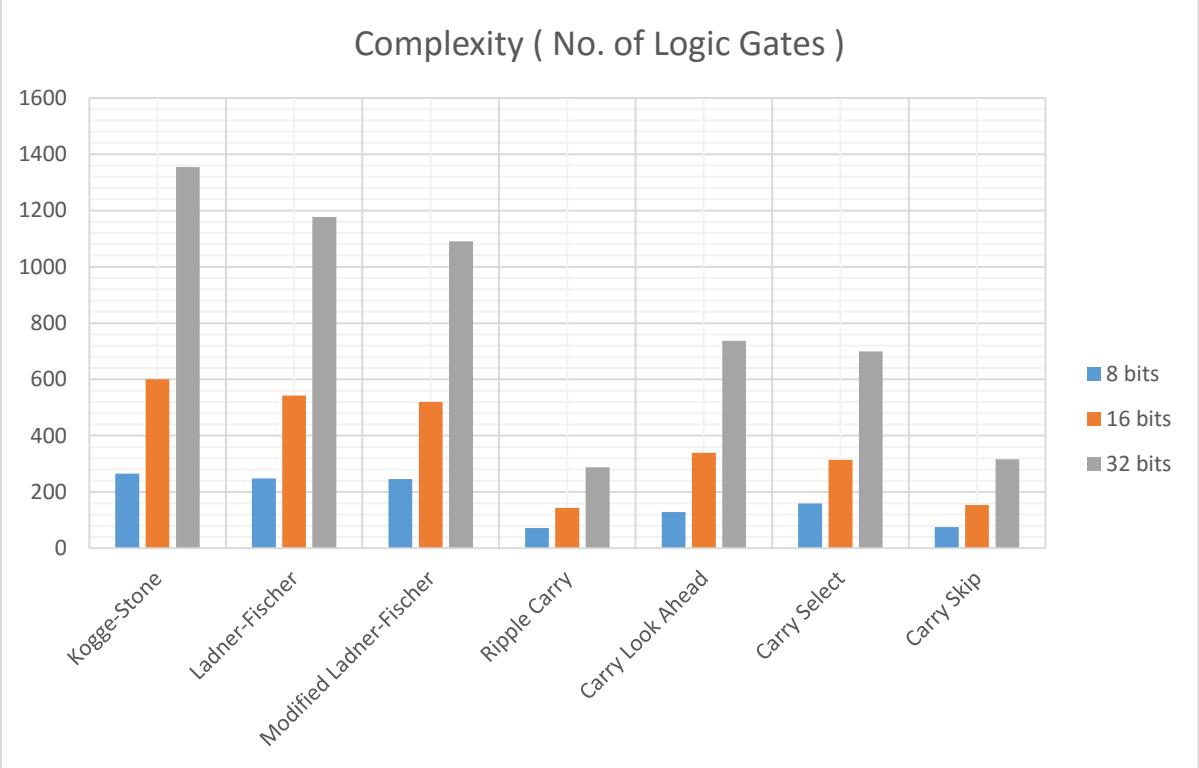

Fig 9: Complexity Comparison for the Adder Topologies for 8, 16 and 32 Bit Sizes

Chapter 5: Design of Adder Operating in the Subthreshold Region

In certain emerging applications, energy efficiency is considered over the traditional emphasis on timing. The circuits designed for these applications can be operated at much reduced performance levels in order to lengthen their battery lifetimes. These ultra-low power circuits consume minimum energy since they operate in the sub-threshold region, where the power supply voltage is below the device threshold voltage.

Since the Kogge-Stone Adder is the fastest adder topology as per the delay comparison results investigated in this work, it was decided to implement this circuit in the Sub threshold region.

The 8-bit configuration was chosen keeping in mind the noise margin and exponential delay increase seen in the sub-threshold region with increasing complexity of the circuit.

5.1 Characterization of Standard Cells for Operation in the Subthreshold Region

There is a need to characterize the standard cells for sub threshold operation to understand the performance of the adder circuit that will be implemented.

The threshold voltage of the NMOS and PMOS models used in the CMOS implementation of the standard cells was 0.45V. A voltage of 0.2V (<0.45V) was chosen as the supply voltage for the Kogge-Stone Adder. Using SPICE Simulations, the rise and fall delay and transition values were calculated for the NAND, NOR and INV cells. These values were tabulated in terms of the two dimensional tables in terms of input transition and output capacitance load.

An example of the characterization table for the INVX1 cell based on input transition and output capacitance load is shown in Fig. 10.

ndex	Cap load	i/p Transition	r_delay	f_delay	r_transition	f_transition
1	1.00E-13	1.00E-10	5.99E-07	5.33E-07	1.25E-06	1.06E-06
2	1.00E-13	1.00E-09	6.00E-07	5.34E-07	1.25E-06	1.06E-06
3	1.00E-13	1.00E-08	6.02E-07	5.36E-07	1.25E-06	1.06E-06
4	1.00E-13	1.00E-07	6.28E-07	5.60E-07	1.25E-06	1.06E-06
5	1.00E-13	1.00E-06	8.96E-07	8.25E-07	1.29E-06	1.11E-06
6	1.00E-13	1.00E-05	2.98E-06	2.66E-06	4.07E-06	4.05E-06
7	2.00E-13	1.00E-10	1.19E-06	1.06E-06	2.49E-06	2.10E-06
8	2.00E-13	1.00E-09	1.19E-06	1.06E-06	2.49E-06	2.10E-06
9	2.00E-13	1.00E-08	1.19E-06	1.06E-06	2.49E-06	2.10E-06
10	2.00E-13	1.00E-07	1.21E-06	1.09E-06	2.48E-06	2.10E-06
11	2.00E-13	1.00E-06	1.48E-06	1.35E-06	2.49E-06	2.10E-06
12	2.00E-13	1.00E-05	4.07E-06	3.78E-06	4.71E-06	4.59E-06
13	1.50E-12	1.00E-10	8.84E-06	7.86E-06	1.86E-05	1.57E-05
14	1.50E-12	1.00E-09	8.86E-06	7.85E-06	1.85E-05	1.56E-05
15	1.50E-12	1.00E-08	8.84E-06	7.87E-06	1.85E-05	1.57E-05
16	1.50E-12	1.00E-07	8.88E-06	7.89E-06	1.85E-05	1.57E-05
17	1.50E-12	1.00E-06	9.13E-06	8.14E-06	1.86E-05	1.57E-05
18	1.50E-12	1.00E-05	1.18E-05	1.08E-05	1.87E-05	1.59E-05

Fig 10: Characterization Table for INVX1, VDD = 0.2 V

5.2 Subthreshold Implementation

These values were used to generate the sub threshold logical library which was used to design the Kogge-Stone adder topology using Virtuoso Schematic Editor. The waveforms below show the transition of the last sum bit for a given set of inputs. The sub-threshold region waveform is pretty robust, but shows significantly higher delay.

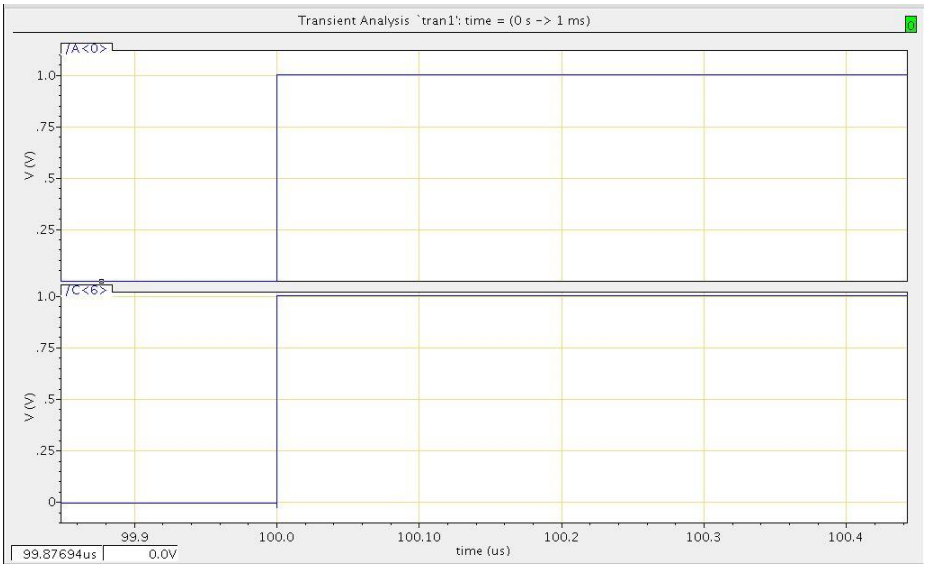

Fig 11: Simulation Waveforms at VDD=1V and T=298K

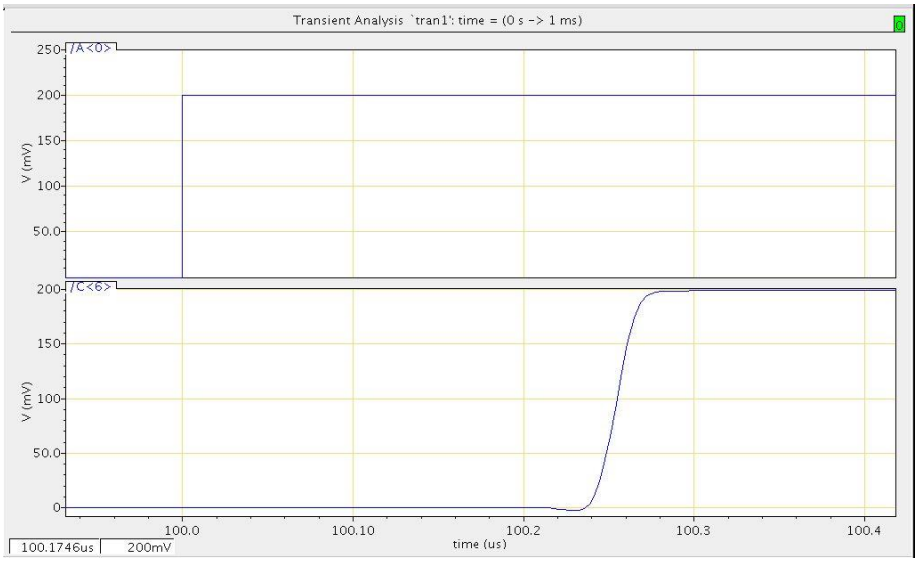

Fig12: Simulation Waveforms at VDD=0.2V and T=298K

Here, A<0-7> and B<0-7> are the input operands. C<0-7> are the sum bits.

5.3 Delay of the Circuit in the Subthreshold Region:

The critical path delay was calculated using static timing analysis with the help of the characterized sub threshold standard cell library.

```
Startpoint: B[5] (input port)
 Endpoint: C[6] (output port)
Path Group: (none)
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
input external delay                           0.00       0.00 r
B[5] (in)                                      0.00       0.00 r
I10/ip1 (gipi_cell)                            0.00       0.00 r
I10/I6/Y (INVX1)                               0.40       0.40 f
I10/I7/Y (NAND2X1)                             0.70       1.10 r
I10/pi (gipi_cell)                             0.00       1.10 r
I8/pi (prefix_block)                           0.00       1.10 r
I8/I2/Y (NAND2X1)                              0.66       1.77 f
I8/I3/Y (NAND2X1)                              0.72       2.49 r
I8/I4/Y (INVX1)                                0.70       3.19 f
I8/Gi_bar (prefix_block)                       0.00       3.19 f
I9/gi_bar (prefix_block)                       0.00       3.19 f
I9/I3/Y (NAND2X1)                              0.72       3.90 r
I9/I4/Y (INVX1)                                0.70       4.60 f
I9/Gi_bar (prefix_block)                       0.00       4.60 f
I96/gi_bar (prefix_block)                      0.00       4.60 f
I96/I3/Y (NAND2X1)                             0.72       5.32 r
I96/I4/Y (INVX1)                               0.70       6.02 f
I96/Gi_bar (prefix_block)                      0.00       6.02 f
I115/Gi_bar (Cin)                              0.00       6.02 f
I115/I1/Y (NAND2X1)                            0.72       6.73 r
I115/Cout (Cin)                                0.00       6.73 r
I120/ip1 (XOR_two_inputs)                      0.00       6.73 r
I120/I0/Y (INVX1)                              0.70       7.43 f
I120/I2/Y (NAND2X1)                            0.71       8.15 r
I120/I4/Y (NAND2X1)                            0.63       8.78 f
I120/op (XOR_two_inputs)                       0.00       8.78 f
C[6] (out)                                     0.00       8.78 f
data arrival time                                         8.78
-----------------------------------------------------------------
(Path is unconstrained)
```

The critical path delay was found to be **8.78 µs** (All delays in µs)

5.4 Energy Calculation and Comparison with Strong Inversion region:

Using HSPICE, average energy was calculated for the given simulation interval for a single transition. The values are tabulated in Table 7.

Table 7: Energy and Delay Comparison between Sub-Vth and Strong Inversion

Kogge Stone 8 bit	**V= 1V**	**V=0.2V**	**Ratio (Sub-Vth/Strong inversion)**
Delay	0.33ns	8.78us	26606
Energy	~10^-13J	~10^-15J	0.01

Chapter 6: Conclusion

The choice of adder topology significantly varies with the desired application needs. The Kogge-Stone adder is the fastest of the topologies contrasted, but is the most complex and consumes maximum power as well. Non-tree adders are a good choice at lower adder widths since they are smaller, less complex and consume much less power while having comparable delays with respect to tree adders. Sub-threshold operation offers a new dimension to design –tradeoff and can be highly useful for energy constrained applications.

The general trends of the results follow that of [15] [16]. The trade-off in performance parameters are as expected for the adder topologies from analysis of their structures. Post-layout delay is slightly more than pre-layout delay and the difference increases as the adder size is increased due to longer and higher number of wires and thus increased interconnect capacitance that is modelled only in post-layout simulation. The increment in delay of the Kogge-Stone adder is the least of all the adders considered. Even though Carry Look Ahead is fastest among Carry Skip, Carry Select, Ripple Carry and itself, the increment in delay is significantly higher than the fastest tree adder i.e., Kogge-Stone and thus the latter is preferred when speed is critical, but with the trade-off of higher average power consumption.

Due to the higher speed of the PPA's, they have greater complexity and area compared to the other adders. Further, by including an extra stage, the 5 stage modified Ladner-Fischer has fewer prefix blocks and thus overall lesser area and complexity. Further, the higher stage Ladner-Fischer becomes useful for wider adders where the fan out becomes an issue with the conventional Ladner-Fischer despite regular buffering. From the pre and post-layout delay comparison, the modified Ladner-Fischer adder proves more useful while at the same time offering lesser area, complexity and power consumption.

Among CLA, RCA, Carry Select and Carry Skip adders, the delay of the RCA as well as its complexity and area nearly doubles for double the adder width.

However, it offers significantly low average and peak power consumption. Since just the 2 input standard cells were used (NAND, NOR and INV), the CLA has a slightly higher area than expected, particularly for higher adder widths and consequently a higher gate count as well. However, its peak and average power consumption is still lower than Carry Select but higher than Carry Skip adders.

The subthreshold region of operation for adders offers a potentially exciting region of research targeted at applications where energy is the primary concern and not performance. As seen, preliminary analysis with average power shows that there can be a significant improvement in the energy consumption if delays on the order of μs can be tolerated.

Appendix

A.1 Physical Layouts of the Adder Topologies (Scale in μm)

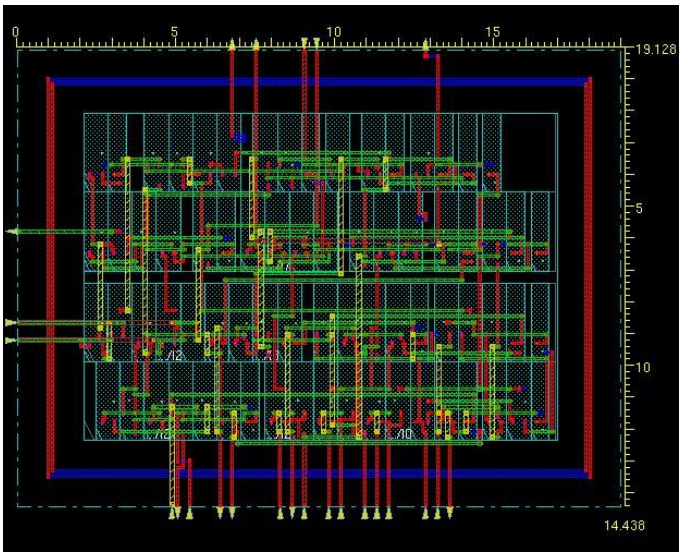

Fig 13.1: Ripple Carry Adder (8-bit)

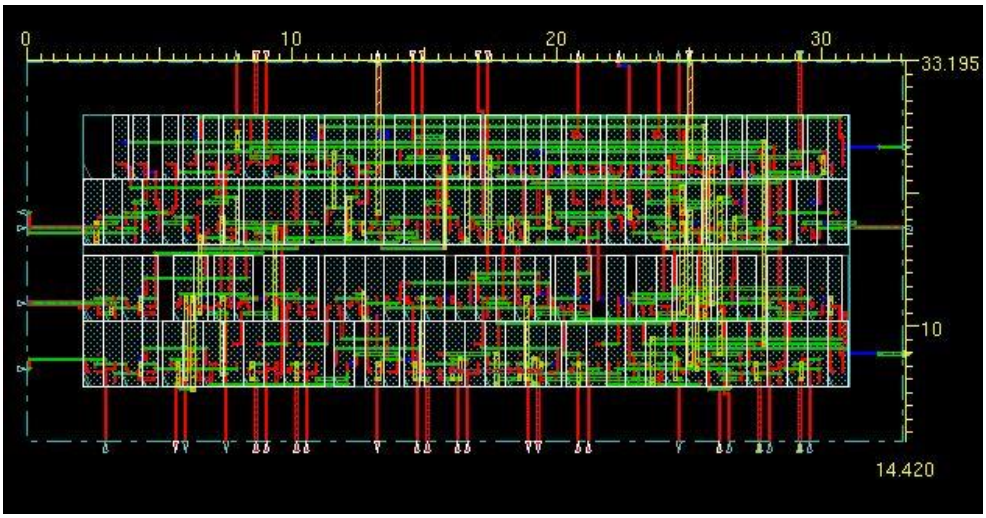

Fig 13.2: Ripple Carry Adder (16-bit)

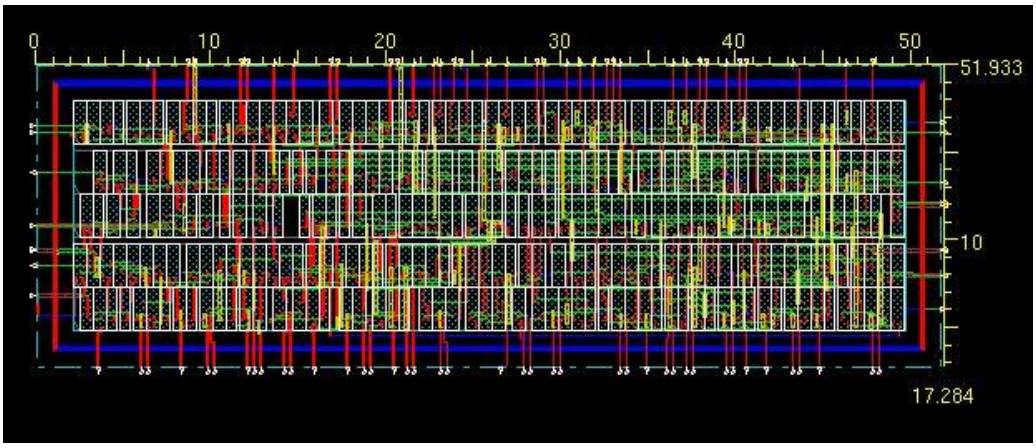

Fig 13.3: Ripple Carry Adder (32-bit)

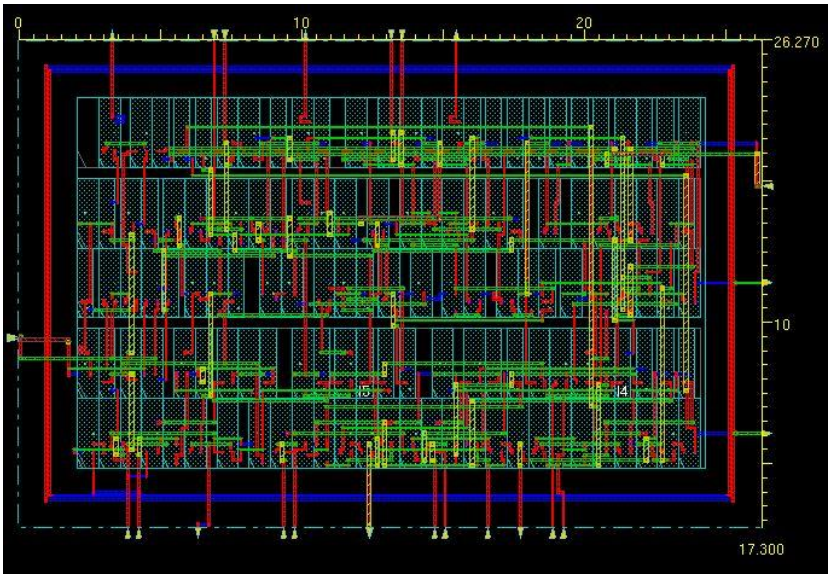

Fig 14.1: Carry Skip Adder (8-bit)

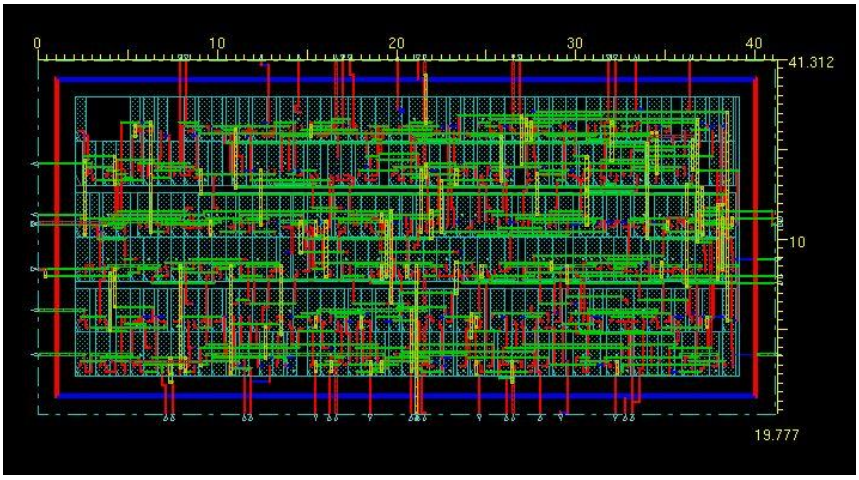

Fig 14.2: Carry Skip Adder (16-bit)

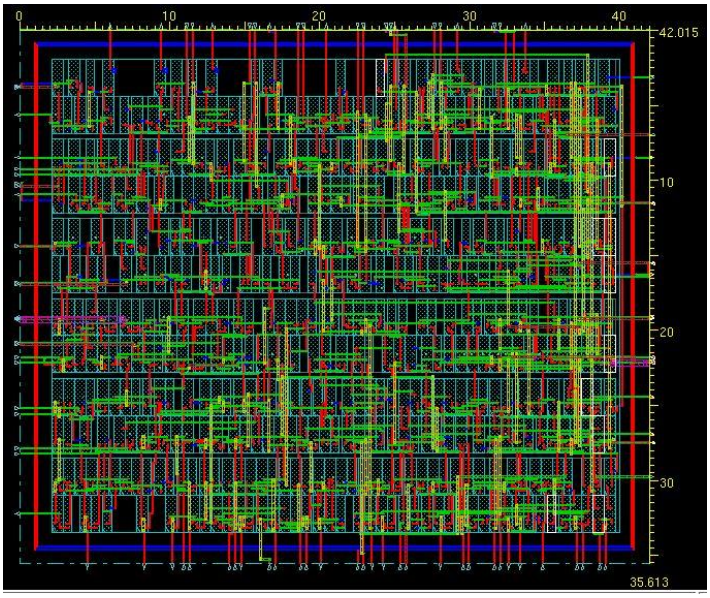

Fig 14.3: Carry Skip Adder (32-bit)

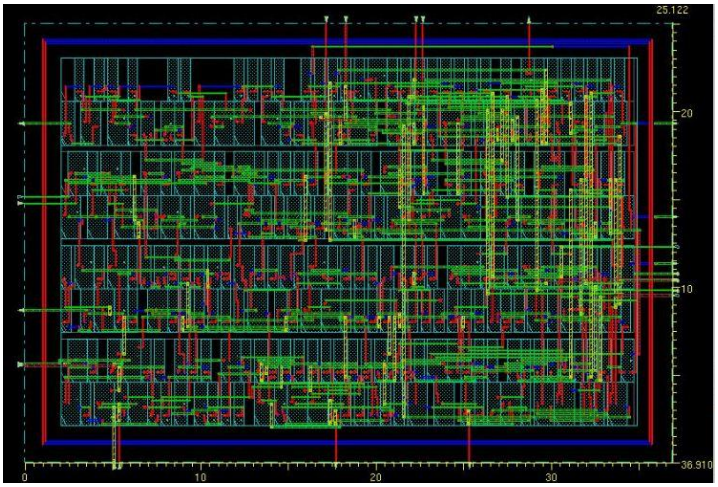

Fig 15.1: Carry Look Ahead Adder (8-bit)

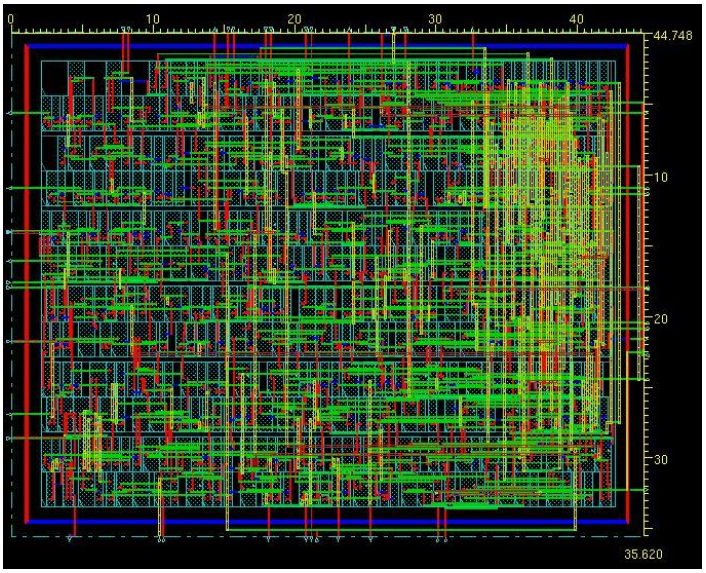

Fig 15.2: Carry-Look Ahead Adder (16-bit)

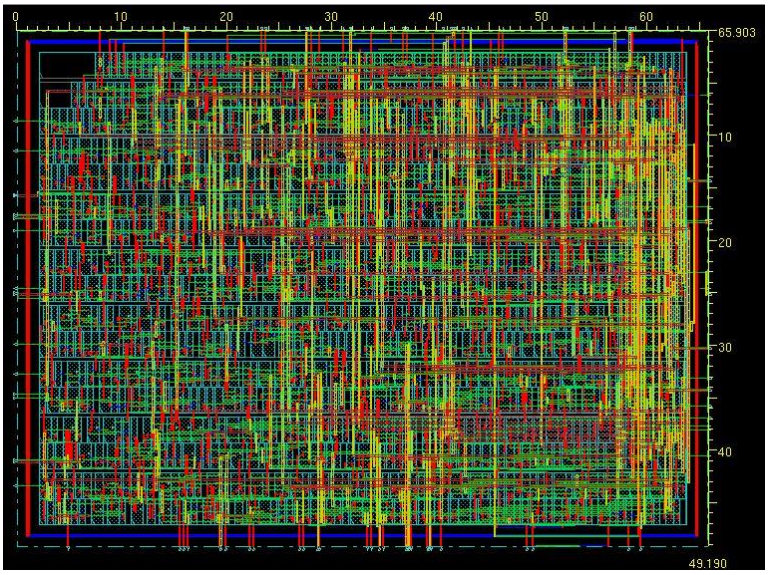

Fig 15.3: Carry-Look Ahead Adder (32-bit)

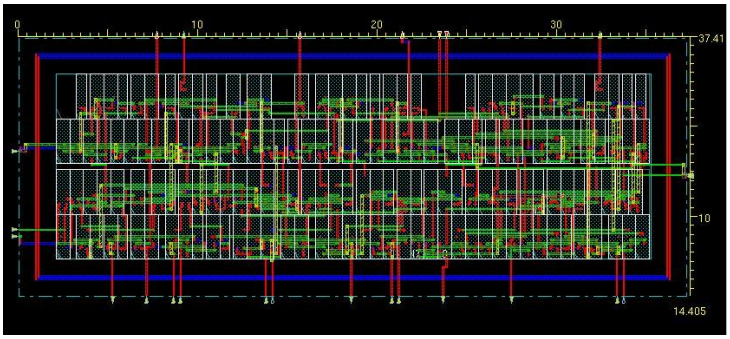

Fig 16.1: Carry Select Adder (8-bit)

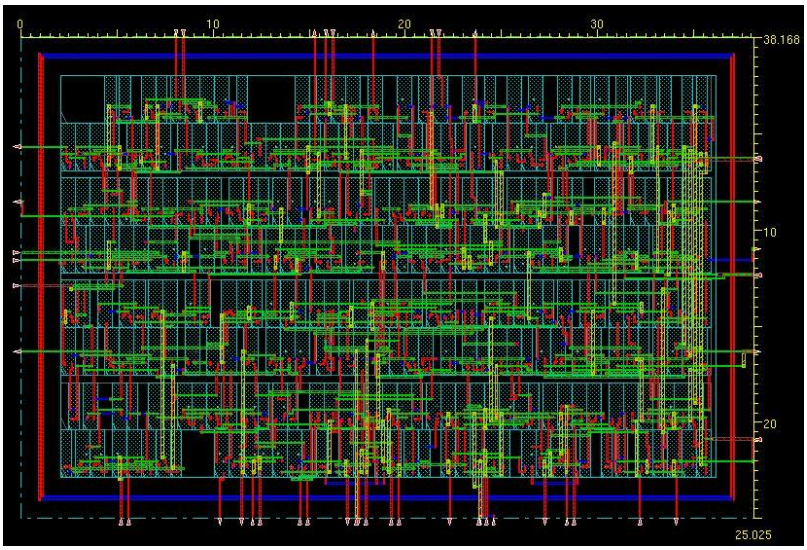

Fig 16.2: Carry Select Adder (16-bit)

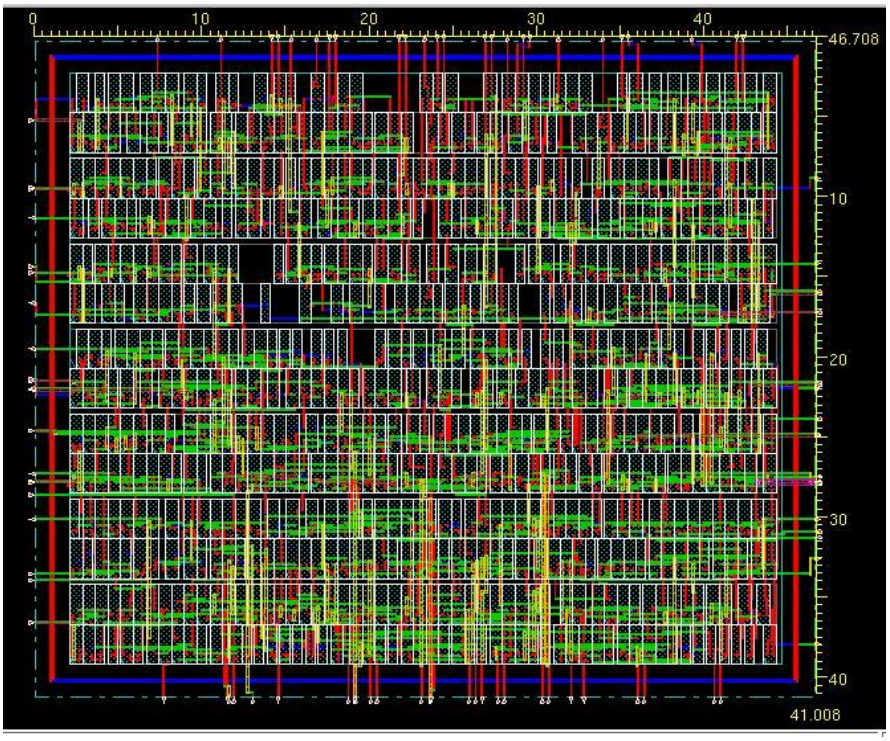

Fig 16.3: Carry Select Adder (32-bit)

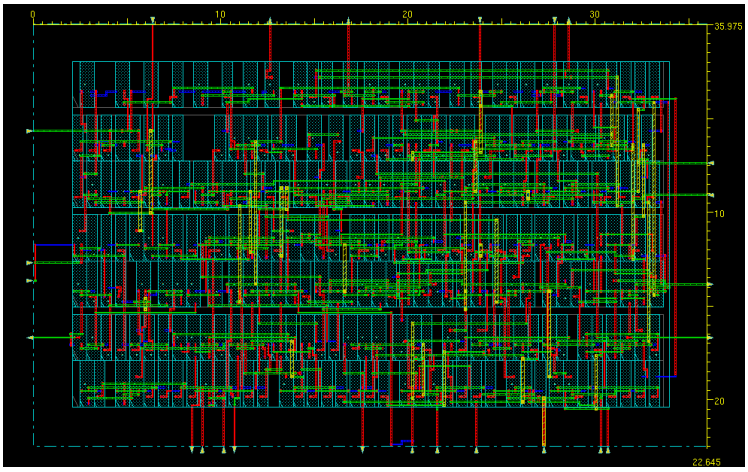

Fig 17.1: Kogge-Stone Adder (8-bit)

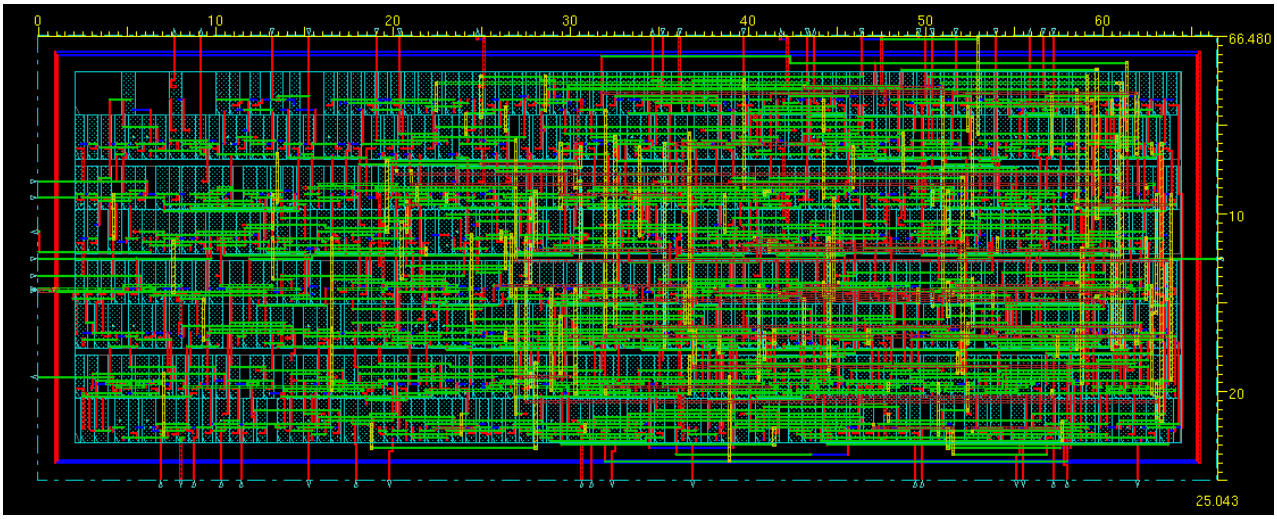

Fig 17.2: Kogge-Stone Adder (16-bit)

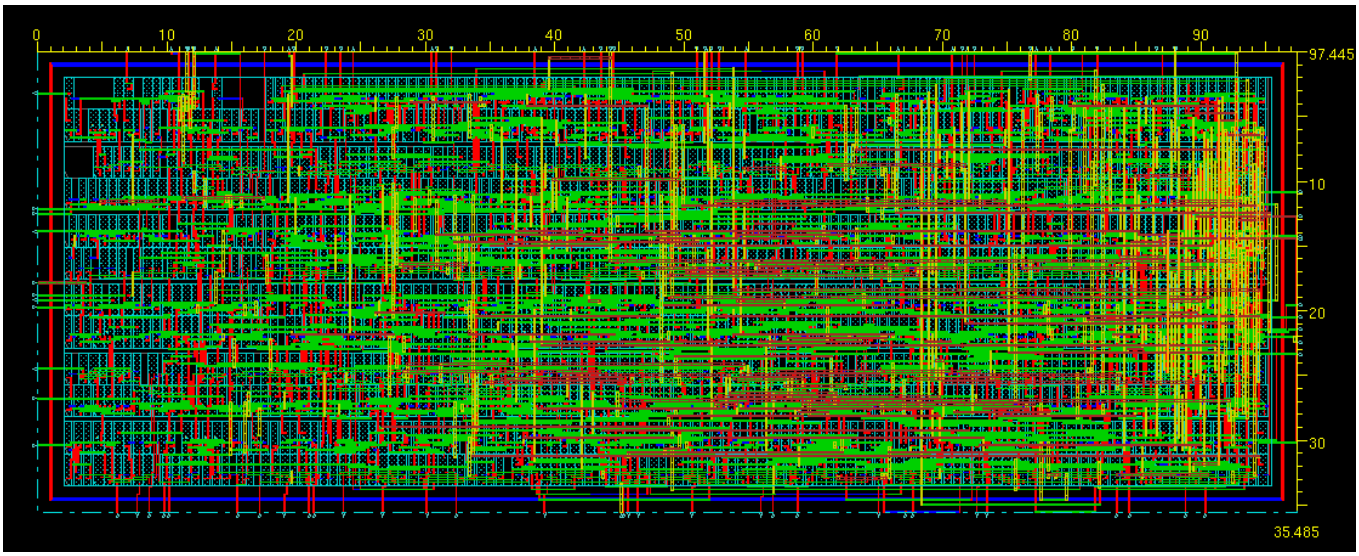

Fig 17.3: Kogge-Stone Adder (32-bit)

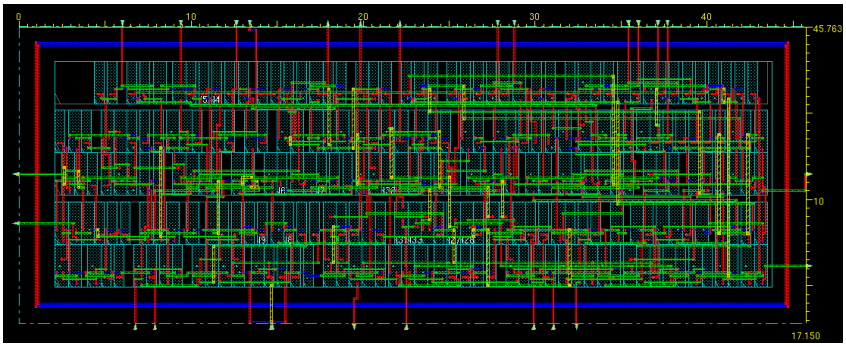

Fig 18.1: Ladner-Fischer Adder (8-bit)

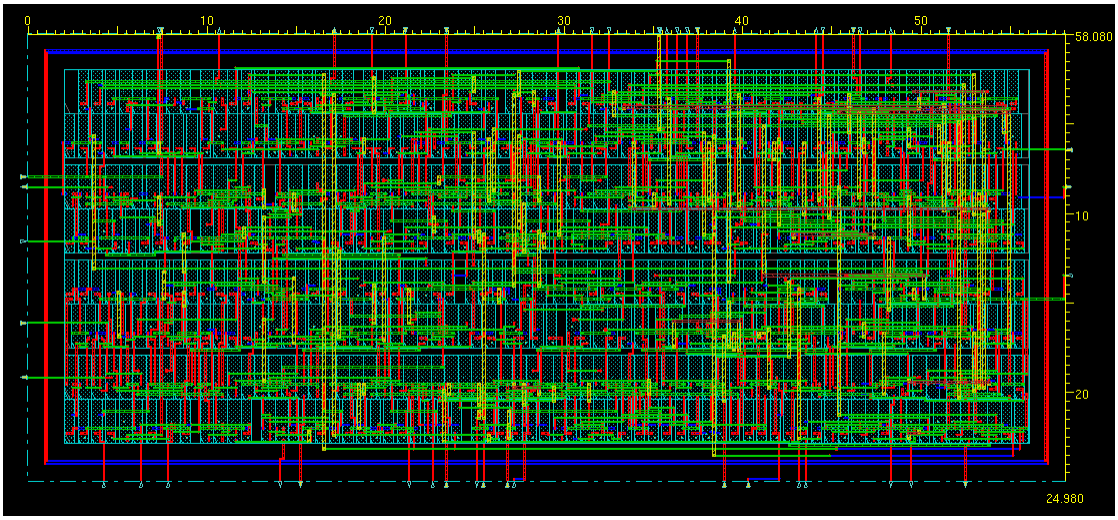

Fig 18.2: Ladner-Fischer Adder (16-bit)

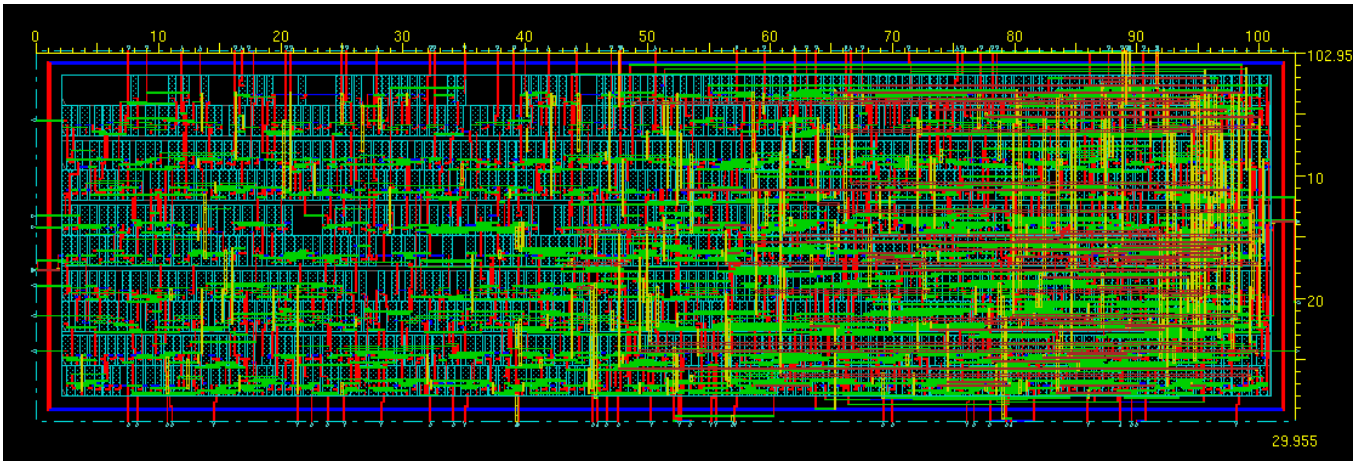

Fig 18.3: Ladner-Fischer Adder (32-bit)

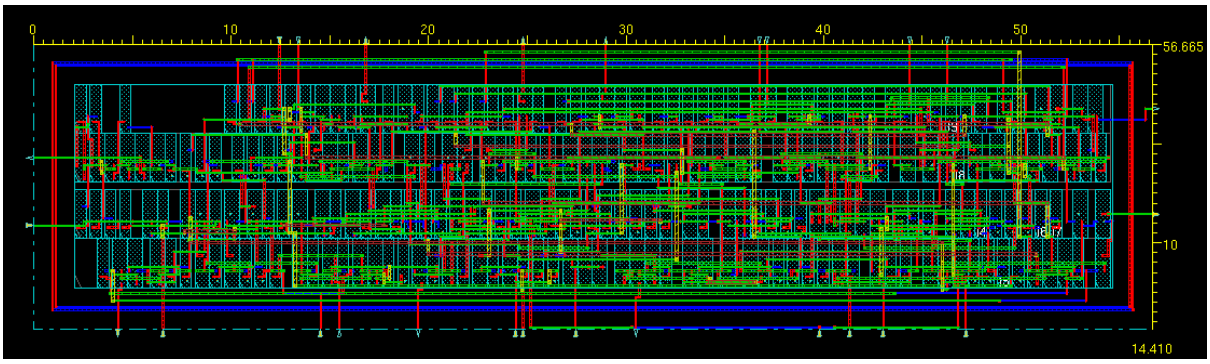

Fig 19.1: Modified Ladner-Fischer Adder (8-bit)

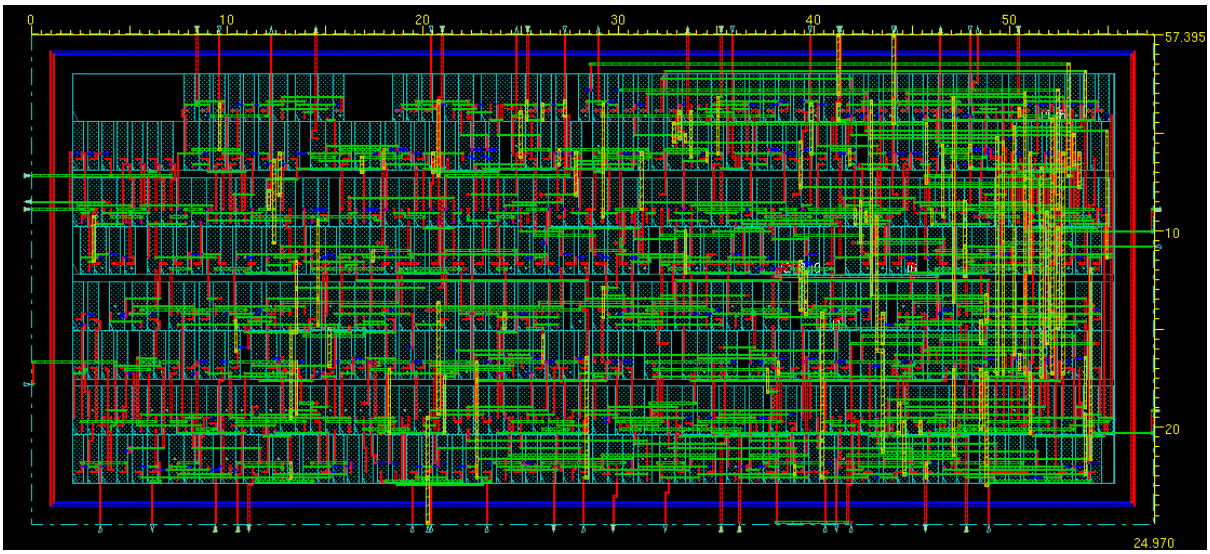

Fig 19.2: Modified Ladner-Fischer Adder (16-bit)

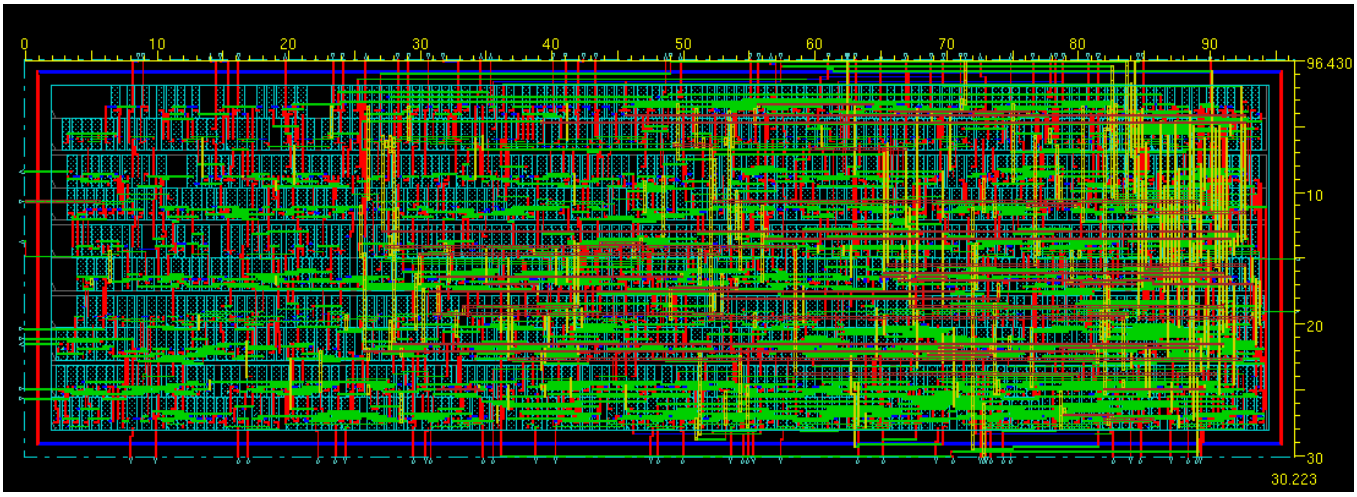

Fig 19.3: Modified Ladner-Fischer Adder (32-bit)

A.2. Post Layout Critical Path Delay Reports from Primetime

A.2.1 Ripple Carry Adder

```
****************************************
Report : timing
       -path_type full
       -delay_type max
       -max_paths 1
Design : RCA_8
Version: F-2011.06-SP1
Date   : Sat Nov 29 11:26:04 2014
****************************************


Startpoint: A[0] (input port)
  Endpoint: COUT (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  A[0] (in)                                0.00 &     0.00 f
  I0/ip1 (FA_9gate)                        0.00 &     0.00 f
  I0/I0/Y (NAND2X1)                        0.03 &     0.03 r
  I0/I1/Y (INVX1)                          0.03 &     0.06 f
  I0/I12/Y (NOR2X1)                        0.04 &     0.10 r
  I0/I6/Y (NAND2X1)                        0.02 &     0.12 f
  I0/I15/Y (NAND2X1)                       0.04 &     0.16 r
```

```
  I0/cout (FA_9gate)                          0.00 &     0.16 r
  I1/cin (FA_9gate)                           0.00 &     0.16 r
  I1/I6/Y (NAND2X1)                           0.03 &     0.19 f
  I1/I15/Y (NAND2X1)                          0.04 &     0.23 r
  I1/cout (FA_9gate)                          0.00 &     0.23 r
  I2/cin (FA_9gate)                           0.00 &     0.23 r
  I2/I6/Y (NAND2X1)                           0.03 &     0.26 f
  I2/I15/Y (NAND2X1)                          0.04 &     0.29 r
  I2/cout (FA_9gate)                          0.00 &     0.29 r
  I3/cin (FA_9gate)                           0.00 &     0.29 r
  I3/I6/Y (NAND2X1)                           0.03 &     0.32 f
  I3/I15/Y (NAND2X1)                          0.04 &     0.36 r
  I3/cout (FA_9gate)                          0.00 &     0.36 r
  I4/cin (FA_9gate)                           0.00 &     0.36 r
  I4/I6/Y (NAND2X1)                           0.03 &     0.39 f
  I4/I15/Y (NAND2X1)                          0.04 &     0.43 r
  I4/cout (FA_9gate)                          0.00 &     0.43 r
  I5/cin (FA_9gate)                           0.00 &     0.43 r
  I5/I6/Y (NAND2X1)                           0.03 &     0.45 f
  I5/I15/Y (NAND2X1)                          0.04 &     0.50 r
  I5/cout (FA_9gate)                          0.00 &     0.50 r
  I6/cin (FA_9gate)                           0.00 &     0.50 r
  I6/I6/Y (NAND2X1)                           0.03 &     0.53 f
  I6/I15/Y (NAND2X1)                          0.04 &     0.57 r
  I6/cout (FA_9gate)                          0.00 &     0.57 r
  I7/cin (FA_9gate)                           0.00 &     0.57 r
  I7/I6/Y (NAND2X1)                           0.03 &     0.60 f
  I7/I15/Y (NAND2X1)                          0.03 &     0.62 r
  I7/cout (FA_9gate)                          0.00 &     0.62 r
  COUT (out)                                  0.00 &     0.62 r
data arrival time                                      0.62
  ---------------------------------------------------------------
  (Path is unconstrained)



****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : RCA_16
Version: F-2011.06-SP1
Date   : Sat Nov 29 14:46:39 2014
****************************************


Startpoint: A[0] (input port)
  Endpoint: COUT (output port)
  Path Group: (none)
  Path Type: max
```

Point	Incr	Path
input external delay	0.00	0.00 f
A[0] (in)	0.00 &	0.00 f
I0/ip1 (FA_9gate)	0.00 &	0.00 f
I0/I0/Y (NAND2X1)	0.03 &	0.03 r
I0/I1/Y (INVX1)	0.03 &	0.06 f
I0/I12/Y (NOR2X1)	0.04 &	0.09 r
I0/I6/Y (NAND2X1)	0.02 &	0.12 f
I0/I15/Y (NAND2X1)	0.04 &	0.16 r
I0/cout (FA_9gate)	0.00 &	0.16 r
I1/cin (FA_9gate)	0.00 &	0.16 r
I1/I6/Y (NAND2X1)	0.03 &	0.18 f
I1/I15/Y (NAND2X1)	0.04 &	0.22 r
I1/cout (FA_9gate)	0.00 &	0.22 r
I2/cin (FA_9gate)	0.00 &	0.22 r
I2/I6/Y (NAND2X1)	0.03 &	0.25 f
I2/I15/Y (NAND2X1)	0.04 &	0.29 r
I2/cout (FA_9gate)	0.00 &	0.29 r
I3/cin (FA_9gate)	0.00 &	0.29 r
I3/I6/Y (NAND2X1)	0.03 &	0.31 f
I3/I15/Y (NAND2X1)	0.04 &	0.35 r
I3/cout (FA_9gate)	0.00 &	0.35 r
I4/cin (FA_9gate)	0.00 &	0.35 r
I4/I6/Y (NAND2X1)	0.03 &	0.38 f
I4/I15/Y (NAND2X1)	0.04 &	0.42 r
I4/cout (FA_9gate)	0.00 &	0.42 r
I5/cin (FA_9gate)	0.00 &	0.42 r
I5/I6/Y (NAND2X1)	0.03 &	0.45 f
I5/I15/Y (NAND2X1)	0.04 &	0.49 r
I5/cout (FA_9gate)	0.00 &	0.49 r
I6/cin (FA_9gate)	0.00 &	0.49 r
I6/I6/Y (NAND2X1)	0.03 &	0.52 f
I6/I15/Y (NAND2X1)	0.04 &	0.56 r
I6/cout (FA_9gate)	0.00 &	0.56 r
I7/cin (FA_9gate)	0.00 &	0.56 r
I7/I6/Y (NAND2X1)	0.03 &	0.59 f
I7/I15/Y (NAND2X1)	0.04 &	0.63 r
I7/cout (FA_9gate)	0.00 &	0.63 r
I10/cin (FA_9gate)	0.00 &	0.63 r
I10/I6/Y (NAND2X1)	0.03 &	0.65 f
I10/I15/Y (NAND2X1)	0.04 &	0.69 r
I10/cout (FA_9gate)	0.00 &	0.69 r
I11/cin (FA_9gate)	0.00 &	0.69 r
I11/I6/Y (NAND2X1)	0.03 &	0.72 f
I11/I15/Y (NAND2X1)	0.04 &	0.76 r
I11/cout (FA_9gate)	0.00 &	0.76 r
I12/cin (FA_9gate)	0.00 &	0.76 r
I12/I6/Y (NAND2X1)	0.03 &	0.79 f
I12/I15/Y (NAND2X1)	0.04 &	0.83 r
I12/cout (FA_9gate)	0.00 &	0.83 r
I13/cin (FA_9gate)	0.00 &	0.83 r
I13/I6/Y (NAND2X1)	0.03 &	0.85 f
I13/I15/Y (NAND2X1)	0.04 &	0.89 r

```
  I13/cout (FA_9gate)                          0.00 &     0.89 r
  I9/cin (FA_9gate)                            0.00 &     0.89 r
  I9/I6/Y (NAND2X1)                            0.03 &     0.92 f
  I9/I15/Y (NAND2X1)                           0.04 &     0.96 r
  I9/cout (FA_9gate)                           0.00 &     0.96 r
  I8/cin (FA_9gate)                            0.00 &     0.96 r
  I8/I6/Y (NAND2X1)                            0.03 &     0.98 f
  I8/I15/Y (NAND2X1)                           0.04 &     1.02 r
  I8/cout (FA_9gate)                           0.00 &     1.02 r
  I15/cin (FA_9gate)                           0.00 &     1.02 r
  I15/I6/Y (NAND2X1)                           0.03 &     1.05 f
  I15/I15/Y (NAND2X1)                          0.04 &     1.09 r
  I15/cout (FA_9gate)                          0.00 &     1.09 r
  I14/cin (FA_9gate)                           0.00 &     1.09 r
  I14/I6/Y (NAND2X1)                           0.03 &     1.11 f
  I14/I15/Y (NAND2X1)                          0.03 &     1.14 r
  I14/cout (FA_9gate)                          0.00 &     1.14 r
  COUT (out)                                   0.00 &     1.14 r
  data arrival time                                       1.14
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : RCA_32
Version: F-2011.06-SP1
Date   : Sat Nov 29 14:38:44 2014
****************************************


Startpoint: A[0] (input port)
  Endpoint: COUT (output port)
  Path Group: (none)
  Path Type: max

  Point                                        Incr       Path
  ---------------------------------------------------------------
  input external delay                         0.00       0.00 f
  A[0] (in)                                    0.00 &     0.00 f
  I0/ip1 (FA_9gate)                            0.00 &     0.00 f
  I0/I0/Y (NAND2X1)                            0.03 &     0.03 r
  I0/I1/Y (INVX1)                              0.03 &     0.06 f
  I0/I12/Y (NOR2X1)                            0.04 &     0.09 r
  I0/I6/Y (NAND2X1)                            0.02 &     0.12 f
  I0/I15/Y (NAND2X1)                           0.04 &     0.16 r
  I0/cout (FA_9gate)                           0.00 &     0.16 r
  I1/cin (FA_9gate)                            0.00 &     0.16 r
  I1/I6/Y (NAND2X1)                            0.03 &     0.19 f
  I1/I15/Y (NAND2X1)                           0.04 &     0.23 r
```

```
I1/cout (FA_9gate)                    0.00 &     0.23 r
I2/cin (FA_9gate)                     0.00 &     0.23 r
I2/I6/Y (NAND2X1)                     0.03 &     0.25 f
I2/I15/Y (NAND2X1)                    0.04 &     0.29 r
I2/cout (FA_9gate)                    0.00 &     0.29 r
I3/cin (FA_9gate)                     0.00 &     0.29 r
I3/I6/Y (NAND2X1)                     0.03 &     0.32 f
I3/I15/Y (NAND2X1)                    0.04 &     0.36 r
I3/cout (FA_9gate)                    0.00 &     0.36 r
I4/cin (FA_9gate)                     0.00 &     0.36 r
I4/I6/Y (NAND2X1)                     0.03 &     0.39 f
I4/I15/Y (NAND2X1)                    0.04 &     0.43 r
I4/cout (FA_9gate)                    0.00 &     0.43 r
I5/cin (FA_9gate)                     0.00 &     0.43 r
I5/I6/Y (NAND2X1)                     0.03 &     0.46 f
I5/I15/Y (NAND2X1)                    0.04 &     0.50 r
I5/cout (FA_9gate)                    0.00 &     0.50 r
I6/cin (FA_9gate)                     0.00 &     0.50 r
I6/I6/Y (NAND2X1)                     0.03 &     0.52 f
I6/I15/Y (NAND2X1)                    0.04 &     0.56 r
I6/cout (FA_9gate)                    0.00 &     0.56 r
I7/cin (FA_9gate)                     0.00 &     0.56 r
I7/I6/Y (NAND2X1)                     0.03 &     0.59 f
I7/I15/Y (NAND2X1)                    0.04 &     0.63 r
I7/cout (FA_9gate)                    0.00 &     0.63 r
I10/cin (FA_9gate)                    0.00 &     0.63 r
I10/I6/Y (NAND2X1)                    0.03 &     0.66 f
I10/I15/Y (NAND2X1)                   0.04 &     0.69 r
I10/cout (FA_9gate)                   0.00 &     0.69 r
I11/cin (FA_9gate)                    0.00 &     0.69 r
I11/I6/Y (NAND2X1)                    0.03 &     0.72 f
I11/I15/Y (NAND2X1)                   0.04 &     0.76 r
I11/cout (FA_9gate)                   0.00 &     0.76 r
I12/cin (FA_9gate)                    0.00 &     0.76 r
I12/I6/Y (NAND2X1)                    0.03 &     0.79 f
I12/I15/Y (NAND2X1)                   0.04 &     0.83 r
I12/cout (FA_9gate)                   0.00 &     0.83 r
I13/cin (FA_9gate)                    0.00 &     0.83 r
I13/I6/Y (NAND2X1)                    0.03 &     0.86 f
I13/I15/Y (NAND2X1)                   0.04 &     0.90 r
I13/cout (FA_9gate)                   0.00 &     0.90 r
I9/cin (FA_9gate)                     0.00 &     0.90 r
I9/I6/Y (NAND2X1)                     0.03 &     0.92 f
I9/I15/Y (NAND2X1)                    0.04 &     0.96 r
I9/cout (FA_9gate)                    0.00 &     0.96 r
I8/cin (FA_9gate)                     0.00 &     0.96 r
I8/I6/Y (NAND2X1)                     0.03 &     0.99 f
I8/I15/Y (NAND2X1)                    0.04 &     1.03 r
I8/cout (FA_9gate)                    0.00 &     1.03 r
I15/cin (FA_9gate)                    0.00 &     1.03 r
I15/I6/Y (NAND2X1)                    0.03 &     1.06 f
I15/I15/Y (NAND2X1)                   0.04 &     1.10 r
I15/cout (FA_9gate)                   0.00 &     1.10 r
I14/cin (FA_9gate)                    0.00 &     1.10 r
```

```
I14/I6/Y (NAND2X1)                      0.03 &     1.13 f
I14/I15/Y (NAND2X1)                     0.04 &     1.17 r
I14/cout (FA_9gate)                     0.00 &     1.17 r
I20/cin (FA_9gate)                      0.00 &     1.17 r
I20/I6/Y (NAND2X1)                      0.03 &     1.20 f
I20/I15/Y (NAND2X1)                     0.04 &     1.24 r
I20/cout (FA_9gate)                     0.00 &     1.24 r
I21/cin (FA_9gate)                      0.00 &     1.24 r
I21/I6/Y (NAND2X1)                      0.03 &     1.27 f
I21/I15/Y (NAND2X1)                     0.04 &     1.31 r
I21/cout (FA_9gate)                     0.00 &     1.31 r
I22/cin (FA_9gate)                      0.00 &     1.31 r
I22/I6/Y (NAND2X1)                      0.03 &     1.34 f
I22/I15/Y (NAND2X1)                     0.04 &     1.38 r
I22/cout (FA_9gate)                     0.00 &     1.38 r
I23/cin (FA_9gate)                      0.00 &     1.38 r
I23/I6/Y (NAND2X1)                      0.03 &     1.41 f
I23/I15/Y (NAND2X1)                     0.04 &     1.45 r
I23/cout (FA_9gate)                     0.00 &     1.45 r
I17/cin (FA_9gate)                      0.00 &     1.45 r
I17/I6/Y (NAND2X1)                      0.03 &     1.48 f
I17/I15/Y (NAND2X1)                     0.04 &     1.52 r
I17/cout (FA_9gate)                     0.00 &     1.52 r
I16/cin (FA_9gate)                      0.00 &     1.52 r
I16/I6/Y (NAND2X1)                      0.03 &     1.55 f
I16/I15/Y (NAND2X1)                     0.04 &     1.59 r
I16/cout (FA_9gate)                     0.00 &     1.59 r
I19/cin (FA_9gate)                      0.00 &     1.59 r
I19/I6/Y (NAND2X1)                      0.03 &     1.61 f
I19/I15/Y (NAND2X1)                     0.04 &     1.66 r
I19/cout (FA_9gate)                     0.00 &     1.66 r
I18/cin (FA_9gate)                      0.00 &     1.66 r
I18/I6/Y (NAND2X1)                      0.03 &     1.68 f
I18/I15/Y (NAND2X1)                     0.04 &     1.72 r
I18/cout (FA_9gate)                     0.00 &     1.72 r
I27/cin (FA_9gate)                      0.00 &     1.72 r
I27/I6/Y (NAND2X1)                      0.03 &     1.75 f
I27/I15/Y (NAND2X1)                     0.04 &     1.79 r
I27/cout (FA_9gate)                     0.00 &     1.79 r
I26/cin (FA_9gate)                      0.00 &     1.79 r
I26/I6/Y (NAND2X1)                      0.03 &     1.81 f
I26/I15/Y (NAND2X1)                     0.04 &     1.85 r
I26/cout (FA_9gate)                     0.00 &     1.85 r
I25/cin (FA_9gate)                      0.00 &     1.85 r
I25/I6/Y (NAND2X1)                      0.03 &     1.88 f
I25/I15/Y (NAND2X1)                     0.04 &     1.92 r
I25/cout (FA_9gate)                     0.00 &     1.92 r
I24/cin (FA_9gate)                      0.00 &     1.92 r
I24/I6/Y (NAND2X1)                      0.03 &     1.95 f
I24/I15/Y (NAND2X1)                     0.04 &     1.98 r
I24/cout (FA_9gate)                     0.00 &     1.98 r
I30/cin (FA_9gate)                      0.00 &     1.98 r
I30/I6/Y (NAND2X1)                      0.03 &     2.01 f
I30/I15/Y (NAND2X1)                     0.04 &     2.05 r
```

```
  I30/cout (FA_9gate)                          0.00 &     2.05 r
  I31/cin (FA_9gate)                           0.00 &     2.05 r
  I31/I6/Y (NAND2X1)                           0.03 &     2.08 f
  I31/I15/Y (NAND2X1)                          0.04 &     2.12 r
  I31/cout (FA_9gate)                          0.00 &     2.12 r
  I28/cin (FA_9gate)                           0.00 &     2.12 r
  I28/I6/Y (NAND2X1)                           0.03 &     2.14 f
  I28/I15/Y (NAND2X1)                          0.04 &     2.18 r
  I28/cout (FA_9gate)                          0.00 &     2.18 r
  I29/cin (FA_9gate)                           0.00 &     2.18 r
  I29/I6/Y (NAND2X1)                           0.03 &     2.21 f
  I29/I15/Y (NAND2X1)                          0.02 &     2.23 r
  I29/cout (FA_9gate)                          0.00 &     2.23 r
  COUT (out)                                   0.00 &     2.23 r
  data arrival time                                       2.23
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.2.2 Carry Skip Adder

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Carry_Skip_8
Version: F-2011.06-SP1
Date   : Sat Nov 29 14:58:25 2014
****************************************


  Startpoint: A[0] (input port clocked by vclk)
  Endpoint: C[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                        Incr       Path
  ---------------------------------------------------------------
  input external delay                         0.00       0.00 f
  A[0] (in)                                    0.00 &     0.00 f
  I3/A[0] (RCA_2bit)                           0.00 &     0.00 f
  I3/I0/ip1 (FA_9gate)                         0.00 &     0.00 f
  I3/I0/I0/Y (NAND2X1)                         0.03 &     0.03 r
  I3/I0/I1/Y (INVX1)                           0.03 &     0.06 f
  I3/I0/I12/Y (NOR2X1)                         0.04 &     0.10 r
  I3/I0/I6/Y (NAND2X1)                         0.02 &     0.12 f
  I3/I0/I15/Y (NAND2X1)                        0.04 &     0.16 r
  I3/I0/cout (FA_9gate)                        0.00 &     0.16 r
  I3/I1/cin (FA_9gate)                         0.00 &     0.16 r
```

```
  I3/I1/I6/Y (NAND2X1)                      0.03 &     0.19 f
  I3/I1/I15/Y (NAND2X1)                     0.03 &     0.22 r
  I3/I1/cout (FA_9gate)                     0.00 &     0.22 r
  I3/COUT (RCA_2bit)                        0.00 &     0.22 r
  I4/Y (INVX1)                              0.03 &     0.25 f
  I0/CIN (RCA_2bit_gipi)                    0.00 &     0.25 f
  I0/I8/Y (NOR2X1)                          0.03 &     0.28 r
  I0/I9/Y (NOR2X1)                          0.02 &     0.30 f
  I0/COUT (RCA_2bit_gipi)                   0.00 &     0.30 f
  I1/CIN (RCA_2bit_gipi)                    0.00 &     0.30 f
  I1/I8/Y (NOR2X1)                          0.03 &     0.33 r
  I1/I9/Y (NOR2X1)                          0.02 &     0.36 f
  I1/COUT (RCA_2bit_gipi)                   0.00 &     0.36 f
  I2/CIN (RCA_2bit_gipi)                    0.00 &     0.36 f
  I2/I13/Y (INVX1)                          0.01 &     0.37 r
  I2/I15/cin (FA_9gate)                     0.00 &     0.37 r
  I2/I15/I6/Y (NAND2X1)                     0.02 &     0.38 f
  I2/I15/I15/Y (NAND2X1)                    0.04 &     0.43 r
  I2/I15/cout (FA_9gate)                    0.00 &     0.43 r
  I2/I14/cin (FA_9gate)                     0.00 &     0.43 r
  I2/I14/I7/Y (NOR2X1)                      0.02 &     0.45 f
  I2/I14/I11/Y (NOR2X1)                     0.02 &     0.47 r
  I2/I14/s (FA_9gate)                       0.00 &     0.47 r
  I2/S[1] (RCA_2bit_gipi)                   0.00 &     0.47 r
  C[7] (out)                                0.00 &     0.47 r
  data arrival time                                    0.47
  ---------------------------------------------------------------


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Carry_Skip_16
Version: F-2011.06-SP1
Date   : Sat Nov 29 15:04:32 2014
****************************************


  Startpoint: A[0] (input port clocked by vclk)
  Endpoint: C[14] (output port)
  Path Group: (none)
  Path Type: max

  Point                                     Incr       Path
  ---------------------------------------------------------------
  input external delay                      0.00       0.00 f
  A[0] (in)                                 0.00 &     0.00 f
  I3/A[0] (RCA_3bit)                        0.00 &     0.00 f
  I3/I0/ip1 (FA_9gate)                      0.00 &     0.00 f
  I3/I0/I0/Y (NAND2X1)                      0.03 &     0.03 r
  I3/I0/I1/Y (INVX1)                        0.03 &     0.06 f
  I3/I0/I12/Y (NOR2X1)                      0.04 &     0.10 r
```

```
  I3/I0/I6/Y (NAND2X1)                    0.02 &     0.12 f
  I3/I0/I15/Y (NAND2X1)                   0.04 &     0.16 r
  I3/I0/cout (FA_9gate)                   0.00 &     0.16 r
  I3/I1/cin (FA_9gate)                    0.00 &     0.16 r
  I3/I1/I6/Y (NAND2X1)                    0.03 &     0.19 f
  I3/I1/I15/Y (NAND2X1)                   0.04 &     0.23 r
  I3/I1/cout (FA_9gate)                   0.00 &     0.23 r
  I3/I2/cin (FA_9gate)                    0.00 &     0.23 r
  I3/I2/I6/Y (NAND2X1)                    0.03 &     0.25 f
  I3/I2/I15/Y (NAND2X1)                   0.03 &     0.28 r
  I3/I2/cout (FA_9gate)                   0.00 &     0.28 r
  I3/COUT (RCA_3bit)                      0.00 &     0.28 r
  I4/Y (INVX1)                            0.03 &     0.31 f
  I8/CIN (RCA_3bit_gipi)                  0.00 &     0.31 f
  I8/I8/Y (NOR2X1)                        0.03 &     0.34 r
  I8/I9/Y (NOR2X1)                        0.02 &     0.37 f
  I8/COUT (RCA_3bit_gipi)                 0.00 &     0.37 f
  I7/CIN (RCA_3bit_gipi)                  0.00 &     0.37 f
  I7/I8/Y (NOR2X1)                        0.03 &     0.40 r
  I7/I9/Y (NOR2X1)                        0.03 &     0.42 f
  I7/COUT (RCA_3bit_gipi)                 0.00 &     0.42 f
  I6/CIN (RCA_3bit_gipi)                  0.00 &     0.42 f
  I6/I8/Y (NOR2X1)                        0.03 &     0.45 r
  I6/I9/Y (NOR2X1)                        0.02 &     0.47 f
  I6/COUT (RCA_3bit_gipi)                 0.00 &     0.47 f
  I9/CIN (RCA_3bit_gipi)                  0.00 &     0.47 f
  I9/I13/Y (INVX1)                        0.01 &     0.48 r
  I9/I10/cin (FA_9gate)                   0.00 &     0.48 r
  I9/I10/I6/Y (NAND2X1)                   0.02 &     0.50 f
  I9/I10/I15/Y (NAND2X1)                  0.04 &     0.54 r
  I9/I10/cout (FA_9gate)                  0.00 &     0.54 r
  I9/I5/cin (FA_9gate)                    0.00 &     0.54 r
  I9/I5/I6/Y (NAND2X1)                    0.03 &     0.57 f
  I9/I5/I15/Y (NAND2X1)                   0.04 &     0.61 r
  I9/I5/cout (FA_9gate)                   0.00 &     0.61 r
  I9/I4/cin (FA_9gate)                    0.00 &     0.61 r
  I9/I4/I7/Y (NOR2X1)                     0.02 &     0.63 f
  I9/I4/I11/Y (NOR2X1)                    0.02 &     0.65 r
  I9/I4/s (FA_9gate)                      0.00 &     0.65 r
  I9/S[2] (RCA_3bit_gipi)                 0.00 &     0.65 r
  C[14] (out)                             0.00 &     0.65 r
  data arrival time                                  0.65
  ---------------------------------------------------------------


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Carry_Skip_32
Version: F-2011.06-SP1
Date   : Sat Nov 29 15:10:02 2014
****************************************
```

```
Startpoint: A[0] (input port clocked by vclk)
Endpoint: COUT (output port)
Path Group: (none)
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
input external delay                           0.00       0.00 f
A[0] (in)                                      0.00 &     0.00 f
I0/A[0] (RCA_4bit)                             0.00 &     0.00 f
I0/I0/ip1 (FA_9gate)                           0.00 &     0.00 f
I0/I0/I0/Y (NAND2X1)                           0.03 &     0.03 r
I0/I0/I1/Y (INVX1)                             0.03 &     0.06 f
I0/I0/I12/Y (NOR2X1)                           0.04 &     0.09 r
I0/I0/I6/Y (NAND2X1)                           0.02 &     0.12 f
I0/I0/I15/Y (NAND2X1)                          0.04 &     0.16 r
I0/I0/cout (FA_9gate)                          0.00 &     0.16 r
I0/I1/cin (FA_9gate)                           0.00 &     0.16 r
I0/I1/I6/Y (NAND2X1)                           0.03 &     0.18 f
I0/I1/I15/Y (NAND2X1)                          0.04 &     0.23 r
I0/I1/cout (FA_9gate)                          0.00 &     0.23 r
I0/I2/cin (FA_9gate)                           0.00 &     0.23 r
I0/I2/I6/Y (NAND2X1)                           0.03 &     0.25 f
I0/I2/I15/Y (NAND2X1)                          0.04 &     0.29 r
I0/I2/cout (FA_9gate)                          0.00 &     0.29 r
I0/I3/cin (FA_9gate)                           0.00 &     0.29 r
I0/I3/I6/Y (NAND2X1)                           0.03 &     0.32 f
I0/I3/I15/Y (NAND2X1)                          0.03 &     0.35 r
I0/I3/cout (FA_9gate)                          0.00 &     0.35 r
I0/COUT (RCA_4bit)                             0.00 &     0.35 r
I8/Y (INVX1)                                   0.03 &     0.38 f
I1/CIN (RCA_4bit_gipi)                         0.00 &     0.38 f
I1/I8/Y (NOR2X1)                               0.03 &     0.41 r
I1/I9/Y (NOR2X1)                               0.03 &     0.43 f
I1/COUT (RCA_4bit_gipi)                        0.00 &     0.43 f
I2/CIN (RCA_4bit_gipi)                         0.00 &     0.43 f
I2/I8/Y (NOR2X1)                               0.03 &     0.47 r
I2/I9/Y (NOR2X1)                               0.03 &     0.49 f
I2/COUT (RCA_4bit_gipi)                        0.00 &     0.49 f
I3/CIN (RCA_4bit_gipi)                         0.00 &     0.49 f
I3/I8/Y (NOR2X1)                               0.03 &     0.52 r
I3/I9/Y (NOR2X1)                               0.02 &     0.55 f
I3/COUT (RCA_4bit_gipi)                        0.00 &     0.55 f
I4/CIN (RCA_4bit_gipi)                         0.00 &     0.55 f
I4/I8/Y (NOR2X1)                               0.03 &     0.58 r
I4/I9/Y (NOR2X1)                               0.03 &     0.60 f
I4/COUT (RCA_4bit_gipi)                        0.00 &     0.60 f
I5/CIN (RCA_4bit_gipi)                         0.00 &     0.60 f
I5/I8/Y (NOR2X1)                               0.03 &     0.64 r
I5/I9/Y (NOR2X1)                               0.02 &     0.66 f
I5/COUT (RCA_4bit_gipi)                        0.00 &     0.66 f
I6/CIN (RCA_4bit_gipi)                         0.00 &     0.66 f
```

```
  I6/I8/Y (NOR2X1)                          0.03 &     0.69 r
  I6/I9/Y (NOR2X1)                          0.02 &     0.71 f
  I6/COUT (RCA_4bit_gipi)                   0.00 &     0.71 f
  I9/Y (INVX1)                              0.01 &     0.72 r
  I7/CIN (RCA_4bit)                         0.00 &     0.72 r
  I7/I0/cin (FA_9gate)                      0.00 &     0.72 r
  I7/I0/I6/Y (NAND2X1)                      0.02 &     0.74 f
  I7/I0/I15/Y (NAND2X1)                     0.04 &     0.78 r
  I7/I0/cout (FA_9gate)                     0.00 &     0.78 r
  I7/I1/cin (FA_9gate)                      0.00 &     0.78 r
  I7/I1/I6/Y (NAND2X1)                      0.03 &     0.80 f
  I7/I1/I15/Y (NAND2X1)                     0.04 &     0.84 r
  I7/I1/cout (FA_9gate)                     0.00 &     0.84 r
  I7/I2/cin (FA_9gate)                      0.00 &     0.84 r
  I7/I2/I6/Y (NAND2X1)                      0.03 &     0.87 f
  I7/I2/I15/Y (NAND2X1)                     0.04 &     0.91 r
  I7/I2/cout (FA_9gate)                     0.00 &     0.91 r
  I7/I3/cin (FA_9gate)                      0.00 &     0.91 r
  I7/I3/I6/Y (NAND2X1)                      0.03 &     0.94 f
  I7/I3/I15/Y (NAND2X1)                     0.02 &     0.96 r
  I7/I3/cout (FA_9gate)                     0.00 &     0.96 r
  I7/COUT (RCA_4bit)                        0.00 &     0.96 r
  COUT (out)                                0.00 &     0.96 r
  data arrival time                                    0.96
  ---------------------------------------------------------------
```

A.2.3 Carry Look Ahead Adder

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : adder
Version: F-2011.06-SP1
Date   : Sat Nov 29 15:44:04 2014
****************************************


  Startpoint: a[2] (input port)
  Endpoint: c[5] (output port)
  Path Group: (none)
  Path Type: max

  Point                                     Incr       Path
  ---------------------------------------------------------------
  input external delay                      0.00       0.00 f
```

```
  a[2] (in)                                0.00 &     0.00 f
  add_5/A[2] (adder_DW01_add_1)            0.00 &     0.00 f
  add_5/U20/Y (AND2X1)                     0.04 &     0.04 f
  add_5/U21/Y (INVX1)                      0.01 &     0.05 r
  add_5/U143/Y (AND2X1)                    0.04 &     0.09 r
  add_5/U144/Y (INVX1)                     0.03 &     0.12 f
  add_5/U207/Y (AND2X1)                    0.03 &     0.15 f
  add_5/U151/Y (AND2X1)                    0.05 &     0.20 f
  add_5/U152/Y (INVX1)                     0.01 &     0.21 r
  add_5/U202/Y (AND2X1)                    0.03 &     0.24 r
  add_5/U41/Y (AND2X1)                     0.04 &     0.28 r
  add_5/U42/Y (INVX1)                      0.02 &     0.30 f
  add_5/U259/Y (NOR2X1)                    0.03 &     0.33 r
  add_5/U61/Y (INVX1)                      0.02 &     0.35 f
  add_5/U62/Y (INVX1)                      0.00 &     0.35 r
  add_5/U258/Y (NOR2X1)                    0.01 &     0.36 f
  add_5/SUM[5] (adder_DW01_add_1)          0.00 &     0.36 f
  c[5] (out)                               0.00 &     0.36 f
  data arrival time                                   0.36
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : adder
Version: F-2011.06-SP1
Date   : Sat Nov 29 15:51:14 2014
****************************************


  Startpoint: a[7] (input port)
  Endpoint: c[10] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  input external delay                     0.00       0.00 f
  a[7] (in)                                0.00 &     0.00 f
  add_5/A[7] (adder_DW01_add_1)            0.00 &     0.00 f
  add_5/U510/Y (INVX1)                     0.02 &     0.02 r
  add_5/U256/Y (AND2X1)                    0.07 &     0.09 r
  add_5/U257/Y (INVX1)                     0.05 &     0.14 f
  add_5/U235/Y (AND2X1)                    0.05 &     0.19 f
  add_5/U236/Y (INVX1)                     0.02 &     0.21 r
  add_5/U59/Y (AND2X1)                     0.04 &     0.26 r
  add_5/U60/Y (INVX1)                      0.02 &     0.28 f
  add_5/U270/Y (AND2X1)                    0.05 &     0.33 f
  add_5/U271/Y (INVX1)                     0.02 &     0.35 r
  add_5/U224/Y (AND2X1)                    0.04 &     0.39 r
```

```
  add_5/U21/Y (INVX1)                      0.03 &     0.42 f
  add_5/U222/Y (AND2X1)                    0.03 &     0.45 f
  add_5/U223/Y (INVX1)                     0.02 &     0.47 r
  add_5/U126/Y (AND2X1)                    0.03 &     0.50 r
  add_5/U127/Y (INVX1)                     0.02 &     0.53 f
  add_5/U403/Y (AND2X1)                    0.03 &     0.56 f
  add_5/U495/Y (NOR2X1)                    0.03 &     0.59 r
  add_5/SUM[10] (adder_DW01_add_1)         0.00 &     0.59 r
  c[10] (out)                              0.00 &     0.59 r
  data arrival time                                   0.59
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : adder
Version: F-2011.06-SP1
Date   : Sat Nov 29 15:58:55 2014
****************************************


  Startpoint: a[15] (input port)
  Endpoint: c[18] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  input external delay                     0.00       0.00 f
  a[15] (in)                               0.00 &     0.00 f
  add_5/A[15] (adder_DW01_add_1)           0.00 &     0.00 f
  add_5/U355/Y (AND2X1)                    0.04 &     0.04 f
  add_5/U356/Y (INVX1)                     0.01 &     0.05 r
  add_5/U407/Y (AND2X1)                    0.04 &     0.09 r
  add_5/U408/Y (INVX1)                     0.02 &     0.11 f
  add_5/U1067/Y (NOR2X1)                   0.03 &     0.14 r
  add_5/U909/Y (INVX1)                     0.02 &     0.16 f
  add_5/U85/Y (AND2X1)                     0.04 &     0.20 f
  add_5/U572/Y (INVX1)                     0.01 &     0.21 r
  add_5/U426/Y (AND2X1)                    0.04 &     0.25 r
  add_5/U427/Y (INVX1)                     0.03 &     0.27 f
  add_5/U860/Y (INVX1)                     0.00 &     0.28 r
  add_5/U405/Y (AND2X1)                    0.03 &     0.31 r
  add_5/U406/Y (INVX1)                     0.02 &     0.33 f
  add_5/U1065/Y (NOR2X1)                   0.03 &     0.36 r
  add_5/U170/Y (INVX1)                     0.02 &     0.38 f
  add_5/U171/Y (INVX1)                     0.00 &     0.38 r
  add_5/U79/Y (AND2X1)                     0.08 &     0.47 r
  add_5/U1051/Y (NOR2X1)                   0.05 &     0.52 f
```

```
  add_5/U403/Y (INVX1)                     0.00 &     0.53 r
  add_5/U404/Y (INVX1)                     0.02 &     0.55 f
  add_5/U881/Y (NOR2X1)                    0.06 &     0.60 r
  add_5/U890/Y (INVX1)                     0.06 &     0.66 f
  add_5/U1050/Y (NOR2X1)                   0.06 &     0.73 r
  add_5/U401/Y (INVX1)                     0.04 &     0.77 f
  add_5/U402/Y (INVX1)                     0.04 &     0.81 r
  add_5/U1048/Y (NOR2X1)                   0.02 &     0.83 f
  add_5/SUM[18] (adder_DW01_add_1)         0.00 &     0.83 f
  c[18] (out)                              0.00 &     0.83 f
  data arrival time                                   0.83
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.2.4 Carry Select Adder

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Carry_Select_8
Version: F-2011.06-SP1
Date   : Sat Nov 29 02:49:47 2014
****************************************


  Startpoint: A[2] (input port clocked by vclk)
  Endpoint: C[6] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  A[2] (in)                                0.00 &     0.00 f
  I2/A[0] (RCA_3bit)                       0.00 &     0.00 f
  I2/I0/ip1 (FA_9gate)                     0.00 &     0.00 f
  I2/I0/I0/Y (NAND2X1)                     0.03 &     0.03 r
  I2/I0/I1/Y (INVX1)                       0.03 H     0.06 f
  I2/I0/I12/Y (NOR2X1)                     0.04       0.09 r
  I2/I0/I6/Y (NAND2X1)                     0.02 H     0.11 f
  I2/I0/I15/Y (NAND2X1)                    0.03 &     0.14 r
  I2/I0/cout (FA_9gate)                    0.00 &     0.14 r
  I2/I1/cin (FA_9gate)                     0.00 &     0.14 r
  I2/I1/I6/Y (NAND2X1)                     0.03 &     0.17 f
  I2/I1/I15/Y (NAND2X1)                    0.04 &     0.21 r
  I2/I1/cout (FA_9gate)                    0.00 &     0.21 r
  I2/I2/cin (FA_9gate)                     0.00 &     0.21 r
  I2/I2/I6/Y (NAND2X1)                     0.03 &     0.24 f
```

```
  I2/I2/I15/Y (NAND2X1)                    0.03 &     0.27 r
  I2/I2/cout (FA_9gate)                    0.00 &     0.27 r
  I2/COUT (RCA_3bit)                       0.00 &     0.27 r
  I13/Y (NAND2X1)                          0.02 &     0.29 f
  I12/Y (NAND2X1)                          0.05 &     0.34 r
  I6/sel (Mux_2_to_1_3copies)              0.00 &     0.34 r
  I6/I0/Y (INVX4)                          0.03 &     0.36 f
  I6/I10/Y (NAND2X1)                       0.03 &     0.40 r
  I6/I8/Y (NAND2X1)                        0.02 &     0.41 f
  I6/s[1] (Mux_2_to_1_3copies)             0.00 &     0.41 f
  C[6] (out)                               0.00 &     0.41 f
  data arrival time                                   0.41
  ---------------------------------------------------------------
  (Path is unconstrained)



****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Carry_Select_16
Version: F-2011.06-SP1
Date   : Sat Nov 29 10:58:08 2014
****************************************


  Startpoint: A[0] (input port clocked by vclk)
  Endpoint: C[12] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  input external delay                     0.00       0.00 f
  A[0] (in)                                0.00 &     0.00 f
  I0/A[0] (RCA_4bit)                       0.00 &     0.00 f
  I0/I0/ip1 (FA_9gate)                     0.00 &     0.00 f
  I0/I0/I0/Y (NAND2X1)                     0.03 &     0.03 r
  I0/I0/I1/Y (INVX1)                       0.03 &     0.06 f
  I0/I0/I12/Y (NOR2X1)                     0.04 &     0.09 r
  I0/I0/I6/Y (NAND2X1)                     0.02 &     0.12 f
  I0/I0/I15/Y (NAND2X1)                    0.04 &     0.16 r
  I0/I0/cout (FA_9gate)                    0.00 &     0.16 r
  I0/I1/cin (FA_9gate)                     0.00 &     0.16 r
  I0/I1/I6/Y (NAND2X1)                     0.03 &     0.18 f
  I0/I1/I15/Y (NAND2X1)                    0.04 &     0.22 r
  I0/I1/cout (FA_9gate)                    0.00 &     0.22 r
  I0/I2/cin (FA_9gate)                     0.00 &     0.22 r
  I0/I2/I6/Y (NAND2X1)                     0.03 &     0.25 f
  I0/I2/I15/Y (NAND2X1)                    0.04 &     0.29 r
  I0/I2/cout (FA_9gate)                    0.00 &     0.29 r
  I0/I3/cin (FA_9gate)                     0.00 &     0.29 r
```

```
  I0/I3/I6/Y (NAND2X1)                    0.03 &     0.31 f
  I0/I3/I15/Y (NAND2X1)                   0.05 &     0.36 r
  I0/I3/cout (FA_9gate)                   0.00 &     0.36 r
  I0/COUT (RCA_4bit)                      0.00 &     0.36 r
  I10/Y (NAND2X1)                         0.02 &     0.39 f
  I11/Y (NAND2X1)                         0.05 &     0.44 r
  I13/Y (NAND2X1)                         0.03 &     0.47 f
  I12/Y (NAND2X1)                         0.05 &     0.51 r
  I9/sel (Mux_2_to_1_4copies)             0.00 &     0.51 r
  I9/I16/Y (INVX4)                        0.03 &     0.54 f
  I9/I13/Y (NAND2X1)                      0.03 &     0.58 r
  I9/I15/Y (NAND2X1)                      0.02 &     0.60 f
  I9/s[0] (Mux_2_to_1_4copies)            0.00 &     0.60 f
  C[12] (out)                             0.00 &     0.60 f
  data arrival time                                  0.60
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Carry_Select_32
Version: F-2011.06-SP1
Date   : Sat Nov 29 11:28:48 2014
****************************************


Startpoint: A[2] (input port clocked by vclk)
  Endpoint: C[27] (output port)
  Path Group: (none)
  Path Type: max

  Point                                   Incr       Path
  -----------------------------------------------------------
  input external delay                    0.00       0.00 f
  A[2] (in)                               0.00 &     0.00 f
  I29/A[0] (RCA_6bit)                     0.00 &     0.00 f
  I29/I0/ip1 (FA_9gate)                   0.00 &     0.00 f
  I29/I0/I0/Y (NAND2X1)                   0.03 &     0.03 r
  I29/I0/I1/Y (INVX1)                     0.03 &     0.06 f
  I29/I0/I12/Y (NOR2X1)                   0.04 &     0.09 r
  I29/I0/I6/Y (NAND2X1)                   0.02 &     0.12 f
  I29/I0/I15/Y (NAND2X1)                  0.03 &     0.15 r
  I29/I0/cout (FA_9gate)                  0.00 &     0.15 r
  I29/I1/cin (FA_9gate)                   0.00 &     0.15 r
  I29/I1/I6/Y (NAND2X1)                   0.03 &     0.18 f
  I29/I1/I15/Y (NAND2X1)                  0.04 &     0.22 r
  I29/I1/cout (FA_9gate)                  0.00 &     0.22 r
  I29/I2/cin (FA_9gate)                   0.00 &     0.22 r
  I29/I2/I6/Y (NAND2X1)                   0.03 &     0.25 f
  I29/I2/I15/Y (NAND2X1)                  0.04 &     0.29 r
```

```
  I29/I2/cout (FA_9gate)                    0.00 &     0.29 r
  I29/I3/cin (FA_9gate)                     0.00 &     0.29 r
  I29/I3/I6/Y (NAND2X1)                     0.03 &     0.32 f
  I29/I3/I15/Y (NAND2X1)                    0.04 &     0.36 r
  I29/I3/cout (FA_9gate)                    0.00 &     0.36 r
  I29/I4/cin (FA_9gate)                     0.00 &     0.36 r
  I29/I4/I6/Y (NAND2X1)                     0.03 &     0.38 f
  I29/I4/I15/Y (NAND2X1)                    0.04 &     0.42 r
  I29/I4/cout (FA_9gate)                    0.00 &     0.42 r
  I29/I5/cin (FA_9gate)                     0.00 &     0.42 r
  I29/I5/I6/Y (NAND2X1)                     0.03 &     0.45 f
  I29/I5/I15/Y (NAND2X1)                    0.03 &     0.48 r
  I29/I5/cout (FA_9gate)                    0.00 &     0.48 r
  I29/COUT (RCA_6bit)                       0.00 &     0.48 r
  I10/Y (NAND2X1)                           0.02 &     0.50 f
  I11/Y (NAND2X1)                           0.05 &     0.55 r
  I13/Y (NAND2X1)                           0.02 &     0.57 f
  I12/Y (NAND2X1)                           0.05 &     0.62 r
  I18/Y (NAND2X1)                           0.03 &     0.65 f
  I19/Y (NAND2X1)                           0.05 &     0.69 r
  I36/Y (NAND2X1)                           0.02 &     0.72 f
  I37/Y (NAND2X1)                           0.05 &     0.77 r
  I35/sel (Mux_2_to_1_6copies)              0.00 &     0.77 r
  I35/I16/Y (INVX4)                         0.03 &     0.80 f
  I35/I10/Y (NAND2X1)                       0.04 &     0.83 r
  I35/I8/Y (NAND2X1)                        0.02 &     0.85 f
  I35/s[1] (Mux_2_to_1_6copies)             0.00 &     0.85 f
  C[27] (out)                               0.00 &     0.85 f
  data arrival time                                    0.85
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.2.5 Kogge-Stone Adder

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Kogge_8
Version: F-2011.06-SP1
Date   : Fri Nov 28 00:22:49 2014
****************************************


  Startpoint: A[2] (input port clocked by vclk)
  Endpoint: C[7] (output port)
  Path Group: (none)
  Path Type: max


Point                                   Incr       Path
```

```
  ---------------------------------------------------------------
  input external delay                    0.00       0.00 r
  A[2] (in)                               0.00 &     0.00 r
  I35/ip2 (gipi_cell)                     0.00 &     0.00 r
  I35/I5/Y (INVX1)                        0.01 &     0.01 f
  I35/I7/Y (NAND2X1)                      0.04 &     0.06 r
  I35/pi (gipi_cell)                      0.00 &     0.06 r
  I32/pi (prefix_block)                   0.00 &     0.06 r
  I32/I2/Y (NAND2X1)                      0.03 &     0.08 f
  I32/I3/Y (NAND2X1)                      0.03 &     0.12 r
  I32/I4/Y (INVX1)                        0.02 &     0.14 f
  I32/Gi_bar (prefix_block)               0.00 &     0.14 f
  I33/gi_bar (prefix_block)               0.00 &     0.14 f
  I33/I3/Y (NAND2X1)                      0.02 &     0.17 r
  I33/Gi (prefix_block)                   0.00 &     0.17 r
  I94/g_dash (prefix_block)               0.00 &     0.17 r
  I94/I2/Y (NAND2X1)                      0.02 &     0.19 f
  I94/I3/Y (NAND2X1)                      0.03 &     0.22 r
  I94/I4/Y (INVX1)                        0.02 &     0.24 f
  I94/Gi_bar (prefix_block)               0.00 &     0.24 f
  I110/Gi_bar (Cin)                       0.00 &     0.24 f
  I110/I1/Y (NAND2X1)                     0.02 &     0.26 r
  I110/Cout (Cin)                         0.00 &     0.26 r
  I117/ip1 (XOR_two_inputs)               0.00 &     0.26 r
  I117/I0/Y (INVX1)                       0.02 &     0.28 f
  I117/I2/Y (NAND2X1)                     0.03 &     0.31 r
  I117/I4/Y (NAND2X1)                     0.01 &     0.33 f
  I117/op (XOR_two_inputs)                0.00 &     0.33 f
  C[7] (out)                              0.00 &     0.33 f
  data arrival time                                  0.33
  ---------------------------------------------------------------
  (Path is unconstrained)



****************************************
Report : timing
         -path_type full
         -delay_type max
         -max_paths 1
Design : Kogge_16
Version: F-2011.06-SP1
Date   : Fri Nov 28 01:12:06 2014
****************************************


  Startpoint: A[2] (input port clocked by vclk)
  Endpoint: C[15] (output port)
  Path Group: (none)
  Path Type: max

  Point                                   Incr       Path
  ---------------------------------------------------------------
  input external delay                    0.00       0.00 r
  A[2] (in)                               0.00 &     0.00 r
  I35/ip2 (gipi_cell)                     0.00 &     0.00 r
  I35/I5/Y (INVX1)                        0.02 &     0.02 f
  I35/I7/Y (NAND2X1)                      0.05 &     0.06 r
  I35/pi (gipi_cell)                      0.00 &     0.06 r
```

```
  I32/pi (prefix_block)                    0.00 &     0.06 r
  I32/I2/Y (NAND2X1)                       0.03 &     0.09 f
  I32/I3/Y (NAND2X1)                       0.04 &     0.13 r
  I32/I4/Y (INVX1)                         0.03 &     0.15 f
  I32/Gi_bar (prefix_block)                0.00 &     0.15 f
  I33/gi_bar (prefix_block)                0.00 &     0.15 f
  I33/I3/Y (NAND2X1)                       0.03 &     0.19 r
  I33/Gi (prefix_block)                    0.00 &     0.19 r
  I94/g_dash (prefix_block)                0.00 &     0.19 r
  I94/I2/Y (NAND2X1)                       0.03 &     0.21 f
  I94/I3/Y (NAND2X1)                       0.04 &     0.25 r
  I94/Gi (prefix_block)                    0.00 &     0.25 r
  I104/g_dash (prefix_block)               0.00 &     0.25 r
  I104/I2/Y (NAND2X1)                      0.02 &     0.27 f
  I104/I3/Y (NAND2X1)                      0.03 &     0.30 r
  I104/I4/Y (INVX1)                        0.02 &     0.33 f
  I104/Gi_bar (prefix_block)               0.00 &     0.33 f
  I133/Gi_bar (Cin)                        0.00 &     0.33 f
  I133/I1/Y (NAND2X1)                      0.03 &     0.35 r
  I133/Cout (Cin)                          0.00 &     0.35 r
  I130/ip1 (XOR_two_inputs)                0.00 &     0.35 r
  I130/I0/Y (INVX1)                        0.03 &     0.38 f
  I130/I2/Y (NAND2X1)                      0.03 &     0.41 r
  I130/I4/Y (NAND2X1)                      0.01 &     0.42 f
  I130/op (XOR_two_inputs)                 0.00 &     0.42 f
  C[15] (out)                              0.00 &     0.42 f
  data arrival time                                   0.42
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Kogge_32_second
Version: F-2011.06-SP1
Date   : Fri Nov 28 01:33:37 2014
****************************************


  Startpoint: A[3] (input port clocked by vclk)
  Endpoint: C[30] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  input external delay                     0.00       0.00 r
  A[3] (in)                                0.00 &     0.00 r
  I30/ip2 (gipi_cell)                      0.00 &     0.00 r
  I30/I5/Y (INVX1)                         0.01 &     0.01 f
  I30/I7/Y (NAND2X1)                       0.05 &     0.06 r
  I30/pi (gipi_cell)                       0.00 &     0.06 r
  I27/pi (prefix_block)                    0.00 &     0.06 r
  I27/I2/Y (NAND2X1)                       0.03 &     0.09 f
  I27/I3/Y (NAND2X1)                       0.04 &     0.12 r
  I27/Gi (prefix_block)                    0.00 &     0.12 r
  I9/g_dash (prefix_block)                 0.00 &     0.12 r
```

```
  I9/I2/Y (NAND2X1)                          0.02 &     0.14 f
  I9/I3/Y (NAND2X1)                          0.05 &     0.19 r
  I9/I4/Y (INVX1)                            0.03 &     0.23 f
  I9/Gi_bar (prefix_block)                   0.00 &     0.23 f
  I96/gi_bar (prefix_block)                  0.00 &     0.23 f
  I96/I3/Y (NAND2X1)                         0.03 &     0.26 r
  I96/Gi (prefix_block)                      0.00 &     0.26 r
  I103/g_dash (prefix_block)                 0.00 &     0.26 r
  I103/I2/Y (NAND2X1)                        0.03 &     0.29 f
  I103/I3/Y (NAND2X1)                        0.04 &     0.32 r
  I103/Gi (prefix_block)                     0.00 &     0.32 r
  I427/g_dash (prefix_block)                 0.00 &     0.32 r
  I427/I2/Y (NAND2X1)                        0.02 &     0.35 f
  I427/I3/Y (NAND2X1)                        0.03 &     0.37 r
  I427/I4/Y (INVX1)                          0.02 &     0.40 f
  I427/Gi_bar (prefix_block)                 0.00 &     0.40 f
  I2/Gi_bar (Cin)                            0.00 &     0.40 f
  I2/I1/Y (NAND2X1)                          0.02 &     0.42 r
  I2/Cout (Cin)                              0.00 &     0.42 r
  I120/ip1 (XOR_two_inputs)                  0.00 &     0.42 r
  I120/I0/Y (INVX1)                          0.03 &     0.45 f
  I120/I2/Y (NAND2X1)                        0.03 &     0.47 r
  I120/I4/Y (NAND2X1)                        0.01 &     0.49 f
  I120/op (XOR_two_inputs)                   0.00 &     0.49 f
  C[30] (out)                                0.00 &     0.49 f
  data arrival time                                     0.49
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.2.6 Ladner-Fischer Adder

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Ladner_Fisher_8
Version: F-2011.06-SP1
Date   : Fri Nov 28 02:20:10 2014
****************************************


  Startpoint: A[1] (input port clocked by vclk)
  Endpoint: C[6] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  A[1] (in)                                0.00 &     0.00 r
  I40/ip2 (gipi_cell)                      0.00 &     0.00 r
  I40/I5/Y (INVX1)                         0.01 &     0.01 f
  I40/I7/Y (NAND2X1)                       0.03 &     0.05 r
  I40/pi (gipi_cell)                       0.00 &     0.05 r
  I0/pi (prefix_block)                     0.00 &     0.05 r
  I0/I2/Y (NAND2X1)                        0.02 &     0.07 f
```

```
  I0/I3/Y (NAND2X1)                          0.04 &     0.12 r
  I0/Gi (prefix_block)                       0.00 &     0.12 r
  I46/g_dash (prefix_block)                  0.00 &     0.12 r
  I46/I2/Y (NAND2X1)                         0.02 &     0.14 f
  I46/I3/Y (NAND2X1)                         0.04 &     0.18 r
  I46/Gi (prefix_block)                      0.00 &     0.18 r
  I29/Y (INVX1)                              0.03 &     0.21 f
  I28/Y (INVX4)                              0.02 &     0.23 r
  I73/g_dash (prefix_block)                  0.00 &     0.23 r
  I73/I2/Y (NAND2X1)                         0.01 &     0.24 f
  I73/I3/Y (NAND2X1)                         0.03 &     0.27 r
  I73/I4/Y (INVX1)                           0.02 &     0.29 f
  I73/Gi_bar (prefix_block)                  0.00 &     0.29 f
  I139/Gi_bar (Cin)                          0.00 &     0.29 f
  I139/I1/Y (NAND2X1)                        0.02 &     0.31 r
  I139/Cout (Cin)                            0.00 &     0.31 r
  I185/ip1 (XOR_two_inputs)                  0.00 &     0.31 r
  I185/I0/Y (INVX1)                          0.03 &     0.34 f
  I185/I2/Y (NAND2X1)                        0.03 &     0.37 r
  I185/I4/Y (NAND2X1)                        0.01 &     0.38 f
  I185/op (XOR_two_inputs)                   0.00 &     0.38 f
  C[6] (out)                                 0.00 &     0.38 f
  data arrival time                                     0.38
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Ladner_Fisher_16
Version: F-2011.06-SP1
Date   : Fri Nov 28 02:56:53 2014
****************************************


Startpoint: A[1] (input port clocked by vclk)
  Endpoint: C[13] (output port)
  Path Group: (none)
  Path Type: max

  Point                                      Incr       Path
  ---------------------------------------------------------------
  input external delay                       0.00       0.00 r
  A[1] (in)                                  0.00 &     0.00 r
  I88/ip2 (gipi_cell)                        0.00 &     0.00 r
  I88/I5/Y (INVX1)                           0.01 &     0.01 f
  I88/I7/Y (NAND2X1)                         0.03 &     0.05 r
  I88/pi (gipi_cell)                         0.00 &     0.05 r
  I99/pi (prefix_block)                      0.00 &     0.05 r
  I99/I2/Y (NAND2X1)                         0.02 &     0.07 f
  I99/I3/Y (NAND2X1)                         0.05 &     0.12 r
  I99/Gi (prefix_block)                      0.00 &     0.12 r
  I102/g_dash (prefix_block)                 0.00 &     0.12 r
  I102/I2/Y (NAND2X1)                        0.02 &     0.14 f
  I102/I3/Y (NAND2X1)                        0.03 &     0.17 r
  I102/Gi (prefix_block)                     0.00 &     0.17 r
  I112/Y (INVX1)                             0.03 &     0.21 f
```

```
  I110/Y (INVX4)                           0.02 &     0.23 r
  I49/g_dash (prefix_block)                0.00 &     0.23 r
  I49/I2/Y (NAND2X1)                       0.01 &     0.24 f
  I49/I3/Y (NAND2X1)                       0.05 &     0.29 r
  I49/Gi (prefix_block)                    0.00 &     0.29 r
  I292/Y (INVX4)                           0.03 &     0.32 f
  I296/Y (INVX4)                           0.02 &     0.34 r
  I264/g_dash (prefix_block)               0.00 &     0.34 r
  I264/I2/Y (NAND2X1)                      0.01 &     0.35 f
  I264/I3/Y (NAND2X1)                      0.03 &     0.38 r
  I264/I4/Y (INVX1)                        0.02 &     0.41 f
  I264/Gi_bar (prefix_block)               0.00 &     0.41 f
  I275/Gi_bar (Cin)                        0.00 &     0.41 f
  I275/I1/Y (NAND2X1)                      0.03 &     0.44 r
  I275/Cout (Cin)                          0.00 &     0.44 r
  I282/ip1 (XOR_two_inputs)                0.00 &     0.44 r
  I282/I0/Y (INVX1)                        0.03 &     0.47 f
  I282/I2/Y (NAND2X1)                      0.03 &     0.49 r
  I282/I4/Y (NAND2X1)                      0.01 &     0.51 f
  I282/op (XOR_two_inputs)                 0.00 &     0.51 f
  C[13] (out)                              0.00 &     0.51 f
  data arrival time                                   0.51
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Ladner_Fisher_32_extra
Version: F-2011.06-SP1
Date   : Fri Nov 28 11:35:30 2014
****************************************


Startpoint: A[1] (input port clocked by vclk)
  Endpoint: C[18] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  input external delay                     0.00       0.00 r
  A[1] (in)                                0.00 &     0.00 r
  I370/ip2 (gipi_cell)                     0.00 &     0.00 r
  I370/I5/Y (INVX1)                        0.01 &     0.01 f
  I370/I7/Y (NAND2X1)                      0.03 &     0.05 r
  I370/pi (gipi_cell)                      0.00 &     0.05 r
  I251/pi (prefix_block)                   0.00 &     0.05 r
  I251/I2/Y (NAND2X1)                      0.02 &     0.07 f
  I251/I3/Y (NAND2X1)                      0.05 &     0.12 r
  I251/Gi (prefix_block)                   0.00 &     0.12 r
  I209/g_dash (prefix_block)               0.00 &     0.12 r
  I209/I2/Y (NAND2X1)                      0.02 &     0.14 f
  I209/I3/Y (NAND2X1)                      0.03 &     0.17 r
  I209/Gi (prefix_block)                   0.00 &     0.17 r
  I241/Y (INVX1)                           0.03 &     0.21 f
  I225/Y (INVX4)                           0.02 &     0.23 r
```

```
  I192/g_dash (prefix_block)               0.00 &     0.23 r
  I192/I2/Y (NAND2X1)                      0.01 &     0.24 f
  I192/I3/Y (NAND2X1)                      0.10 &     0.34 r
  I192/Gi (prefix_block)                   0.00 &     0.34 r
  I267/g_dash (prefix_block)               0.00 &     0.34 r
  I267/I2/Y (NAND2X1)                      0.04 &     0.39 f
  I267/I3/Y (NAND2X1)                      0.04 &     0.42 r
  I267/Gi (prefix_block)                   0.00 &     0.42 r
  I13/Y (INVX1)                            0.07 &     0.49 f
  I9/Y (INVX4)                             0.04 &     0.53 r
  I599/g_dash (prefix_block)               0.00 &     0.53 r
  I599/I2/Y (NAND2X1)                      0.02 &     0.55 f
  I599/I3/Y (NAND2X1)                      0.03 &     0.58 r
  I599/I4/Y (INVX1)                        0.03 &     0.61 f
  I599/Gi_bar (prefix_block)               0.00 &     0.61 f
  I127/Gi_bar (Cin)                        0.00 &     0.61 f
  I127/I1/Y (NAND2X1)                      0.03 &     0.64 r
  I127/Cout (Cin)                          0.00 &     0.64 r
  I173/ip1 (XOR_two_inputs)                0.00 &     0.64 r
  I173/I0/Y (INVX1)                        0.03 &     0.67 f
  I173/I2/Y (NAND2X1)                      0.03 &     0.70 r
  I173/I4/Y (NAND2X1)                      0.02 &     0.71 f
  I173/op (XOR_two_inputs)                 0.00 &     0.71 f
  C[18] (out)                              0.00 &     0.71 f
  data arrival time                                   0.71
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.2.7 Modified Ladner-Fischer Adder

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Ladner_Fisher_8_MOD
Version: F-2011.06-SP1
Date   : Fri Nov 28 11:59:11 2014
****************************************


Startpoint: A[1] (input port clocked by vclk)
  Endpoint: C[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  A[1] (in)                                0.00 &     0.00 r
  I40/ip2 (gipi_cell)                      0.00 &     0.00 r
  I40/I5/Y (INVX1)                         0.01 &     0.01 f
  I40/I7/Y (NAND2X1)                       0.04 &     0.05 r
  I40/pi (gipi_cell)                       0.00 &     0.05 r
  I0/pi (prefix_block)                     0.00 &     0.05 r
```

```
  I0/I2/Y (NAND2X1)                          0.02 &     0.07 f
  I0/I3/Y (NAND2X1)                          0.04 &     0.11 r
  I0/Gi (prefix_block)                       0.00 &     0.11 r
  I46/g_dash (prefix_block)                  0.00 &     0.11 r
  I46/I2/Y (NAND2X1)                         0.02 &     0.14 f
  I46/I3/Y (NAND2X1)                         0.05 &     0.19 r
  I46/Gi (prefix_block)                      0.00 &     0.19 r
  I73/g_dash (prefix_block)                  0.00 &     0.19 r
  I73/I2/Y (NAND2X1)                         0.03 &     0.21 f
  I73/I3/Y (NAND2X1)                         0.04 &     0.25 r
  I73/Gi (prefix_block)                      0.00 &     0.25 r
  I12/g_dash (prefix_block)                  0.00 &     0.25 r
  I12/I2/Y (NAND2X1)                         0.02 &     0.27 f
  I12/I3/Y (NAND2X1)                         0.03 &     0.30 r
  I12/I4/Y (INVX1)                           0.02 &     0.32 f
  I12/Gi_bar (prefix_block)                  0.00 &     0.32 f
  I138/Gi_bar (Cin)                          0.00 &     0.32 f
  I138/I1/Y (NAND2X1)                        0.02 &     0.34 r
  I138/Cout (Cin)                            0.00 &     0.34 r
  I184/ip1 (XOR_two_inputs)                  0.00 &     0.34 r
  I184/I0/Y (INVX1)                          0.02 &     0.37 f
  I184/I2/Y (NAND2X1)                        0.03 &     0.39 r
  I184/I4/Y (NAND2X1)                        0.02 &     0.41 f
  I184/op (XOR_two_inputs)                   0.00 &     0.41 f
  C[7] (out)                                 0.00 &     0.41 f
  data arrival time                                     0.41
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Ladner_Fisher_16_MOD
Version: F-2011.06-SP1
Date   : Sat Nov 29 01:39:59 2014
****************************************


Startpoint: A[1] (input port clocked by vclk)
  Endpoint: C[15] (output port)
  Path Group: (none)
  Path Type: max

  Point                                      Incr       Path
  ---------------------------------------------------------------
  input external delay                       0.00       0.00 r
  A[1] (in)                                  0.00 &     0.00 r
  I88/ip2 (gipi_cell)                        0.00 &     0.00 r
  I88/I5/Y (INVX1)                           0.01 &     0.01 f
  I88/I7/Y (NAND2X1)                         0.03 &     0.05 r
  I88/pi (gipi_cell)                         0.00 &     0.05 r
  I99/pi (prefix_block)                      0.00 &     0.05 r
  I99/I2/Y (NAND2X1)                         0.02 &     0.07 f
  I99/I3/Y (NAND2X1)                         0.04 &     0.11 r
  I99/Gi (prefix_block)                      0.00 &     0.11 r
```

```
  I102/g_dash (prefix_block)               0.00 &     0.11 r
  I102/I2/Y (NAND2X1)                      0.02 &     0.13 f
  I102/I3/Y (NAND2X1)                      0.05 &     0.19 r
  I102/Gi (prefix_block)                   0.00 &     0.19 r
  I49/g_dash (prefix_block)                0.00 &     0.19 r
  I49/I2/Y (NAND2X1)                       0.03 &     0.21 f
  I49/I3/Y (NAND2X1)                       0.07 &     0.28 r
  I49/Gi (prefix_block)                    0.00 &     0.28 r
  I265/g_dash (prefix_block)               0.00 &     0.28 r
  I265/I2/Y (NAND2X1)                      0.03 &     0.32 f
  I265/I3/Y (NAND2X1)                      0.04 &     0.35 r
  I265/Gi (prefix_block)                   0.00 &     0.35 r
  I10/g_dash (prefix_block)                0.00 &     0.35 r
  I10/I2/Y (NAND2X1)                       0.02 &     0.37 f
  I10/I3/Y (NAND2X1)                       0.03 &     0.40 r
  I10/I4/Y (INVX1)                         0.02 &     0.43 f
  I10/Gi_bar (prefix_block)                0.00 &     0.43 f
  I276/Gi_bar (Cin)                        0.00 &     0.43 f
  I276/I1/Y (NAND2X1)                      0.02 &     0.45 r
  I276/Cout (Cin)                          0.00 &     0.45 r
  I273/ip1 (XOR_two_inputs)                0.00 &     0.45 r
  I273/I0/Y (INVX1)                        0.03 &     0.48 f
  I273/I2/Y (NAND2X1)                      0.03 &     0.50 r
  I273/I4/Y (NAND2X1)                      0.02 &     0.52 f
  I273/op (XOR_two_inputs)                 0.00 &     0.52 f
  C[15] (out)                              0.00 &     0.52 f
  data arrival time                                   0.52
  ---------------------------------------------------------------
  (Path is unconstrained)


****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : Ladner_Fisher_32_MOD
Version: F-2011.06-SP1
Date   : Sat Nov 29 01:51:32 2014
****************************************


Startpoint: A[1] (input port clocked by vclk)
  Endpoint: C[29] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  input external delay                     0.00       0.00 r
  A[1] (in)                                0.00 &     0.00 r
  I88/ip2 (gipi_cell)                      0.00 &     0.00 r
  I88/I5/Y (INVX1)                         0.01 &     0.01 f
  I88/I7/Y (NAND2X1)                       0.03 &     0.05 r
  I88/pi (gipi_cell)                       0.00 &     0.05 r
  I99/pi (prefix_block)                    0.00 &     0.05 r
  I99/I2/Y (NAND2X1)                       0.02 &     0.07 f
  I99/I3/Y (NAND2X1)                       0.04 &     0.11 r
```

```
I99/Gi (prefix_block)                    0.00 &     0.11 r
I102/g_dash (prefix_block)               0.00 &     0.11 r
I102/I2/Y (NAND2X1)                      0.02 &     0.14 f
I102/I3/Y (NAND2X1)                      0.05 &     0.19 r
I102/Gi (prefix_block)                   0.00 &     0.19 r
I49/g_dash (prefix_block)                0.00 &     0.19 r
I49/I2/Y (NAND2X1)                       0.03 &     0.22 f
I49/I3/Y (NAND2X1)                       0.07 &     0.29 r
I49/Gi (prefix_block)                    0.00 &     0.29 r
I267/g_dash (prefix_block)               0.00 &     0.29 r
I267/I2/Y (NAND2X1)                      0.03 &     0.32 f
I267/I3/Y (NAND2X1)                      0.11 &     0.43 r
I267/Gi (prefix_block)                   0.00 &     0.43 r
I590/g_dash (prefix_block)               0.00 &     0.43 r
I590/I2/Y (NAND2X1)                      0.05 &     0.49 f
I590/I3/Y (NAND2X1)                      0.04 &     0.52 r
I590/Gi (prefix_block)                   0.00 &     0.52 r
I70/g_dash (prefix_block)                0.00 &     0.52 r
I70/I2/Y (NAND2X1)                       0.02 &     0.54 f
I70/I3/Y (NAND2X1)                       0.03 &     0.57 r
I70/I4/Y (INVX1)                         0.02 &     0.60 f
I70/Gi_bar (prefix_block)                0.00 &     0.60 f
I116/Gi_bar (Cin)                        0.00 &     0.60 f
I116/I1/Y (NAND2X1)                      0.02 &     0.62 r
I116/Cout (Cin)                          0.00 &     0.62 r
I147/ip1 (XOR_two_inputs)                0.00 &     0.62 r
I147/I0/Y (INVX1)                        0.03 &     0.64 f
I147/I2/Y (NAND2X1)                      0.03 &     0.67 r
I147/I4/Y (NAND2X1)                      0.01 &     0.68 f
I147/op (XOR_two_inputs)                 0.00 &     0.68 f
C[29] (out)                              0.00 &     0.68 f
data arrival time                                   0.68
-----------------------------------------------------------------------
(Path is unconstrained)
```

Bibliography

[1] Gilchrist, B., Pomerene, J. H., and Wong, S. Y., "Fast carry logic for digital computers," *IRE Transactions on Electronic Computers, Vol. 4*, pp. 133-136, 1955.

[2] MacSorley, O. L., "High-speed arithmetic in binary computers," *Proceedings of the IRE, Vol. 49*, pp. 67-91, 1961.

[3] Bedrij, O. J., "Carry-select adder," *IRE Transactions on Electronic Computers, Vol. 3*, pp. 340-346, 1962.

[4] Ladner, R. E., and Fischer, M. J., "Parallel prefix computation," *Journal of the ACM (JACM), Vol. 27*, pp. 831-838, 1980.

[5] Brent, R. P., and Kung, H. T., "A regular layout for parallel adders," *IEEE Transactions on Computers, Vol. 31*, pp. 260-264, 1982.

[6] Kogge, P. M., and Stone, H. S., "A parallel algorithm for the efficient solution of a general class of recurrence equations," *IEEE Transactions on Computers, Vol. 22*, pp. 786-793, 1973.

[7] Knowles, S., "A family of adders," *Proceedings, 14th IEEE Symposium on Computer Arithmetic*, pp. 30-34, 1999.

[8] Guyot, A., Hochet, B., and Muller, J. M., "A way to build efficient carry-skip adders," *IEEE Transactions on Computers, Vol. 36*, pp. 1144-1152, 1987.

[9] Tyagi, A., "A reduced-area scheme for carry-select adders," *IEEE Transactions on Computers, Vol. 42*, pp. 1163-1170, 1993.

[10] B. W. Y. Wei and C. D. Thompson, "Area-time optimal adder designs," *IEEE Transactions on Computers, Vol. 39*, pp. 666-675, 1990.

[11] Callaway, T. K., and Swartzlander, E. E. Jr., “Estimating the power consumption of CMOS adders,” *Proceedings, 11th Symposium on Computer Arithmetic*, pp. 210-216, 1993.

[12] Han, T., and Carlson, D. A., “Fast area-efficient VLSI adders,” *IEEE 8th Symposium on Computer Arithmetic*, pp. 49-56, 1987.

[13] Dao, H. Q., and Oklobdzija, V. G., “Performance comparison of VLSI adders using logical effort,” *Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation*, Berlin: Springer, pp. 23-34, 2002.

[14] Soeleman, H., and Roy, K., “Digital CMOS logic operation in the sub-threshold region,” *Proceedings of the 10th Great Lakes Symposium on VLSI*, pp. 107-112, 2000.

[15] Uma, R., Vijayan, V., Mohanapriya, M., and Paul, S., “Area, delay and power comparison of adder topologies,” *International Journal of VLSI and Communication Systems, Vol. 3, No. 1,* 2012.

[16] Weste, N. H., and Harris, D. M., “*CMOS VLSI design: A Circuits and Systems Perspective*,” India: Pearson Education, 2005.